ESP32-C5

Series SoC Errata Version v1.2

ESPRESSIF

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1 Chip Revision Identification

Espressif is introducing a new **vM.X** numbering scheme to indicate chip revisions. This guide outlines the structure of this scheme and provides information on chip errata and additional identification methods.

1.1 Chip Revision Numbering Scheme

The new numbering scheme **vM.X** consists of the major and minor numbers described below.

M –Major number, indicating the major revision of the chip product. If this number changes, it means the software used for the previous version of the product is incompatible with the new product, and the software version shall be upgraded for the use of the new product.

X –Minor number, indicating the minor revision of the chip product. If this number changes, it means the software used for the previous version of the product is compatible with the new product, and there is no need to upgrade the software.

The **vM.X** scheme replaces previously used chip revision schemes, including ECOx numbers, Vxxx, and other formats if any.

1.2 Primary Identification Methods

eFuse Bits

The chip revision is encoded using two eFuse fields:

- EFUSE_RD_MAC_SYS2_REG[5:4]
- EFUSE_RD_MAC_SYS2_REG[3:0]

Table 1.1: Chip Revision Identification by eFuse Bits

	eFuse Bit	Chip Revision			
		v0.0	v0.1	v1.0	v1.2
Major Number	EFUSE_RD_MAC_SYS2_REG[5]	0	0	0	0
	EFUSE_RD_MAC_SYS2_REG[4]	0	0	1	1
Minor Number	EFUSE_RD_MAC_SYS2_REG[3]	0	0	0	0
	EFUSE_RD_MAC_SYS2_REG[2]	0	0	0	0
	EFUSE_RD_MAC_SYS2_REG[1]	0	0	0	1
	EFUSE_RD_MAC_SYS2_REG[0]	0	1	0	0

Chip Marking

- **Manufacturing Code** line in chip marking

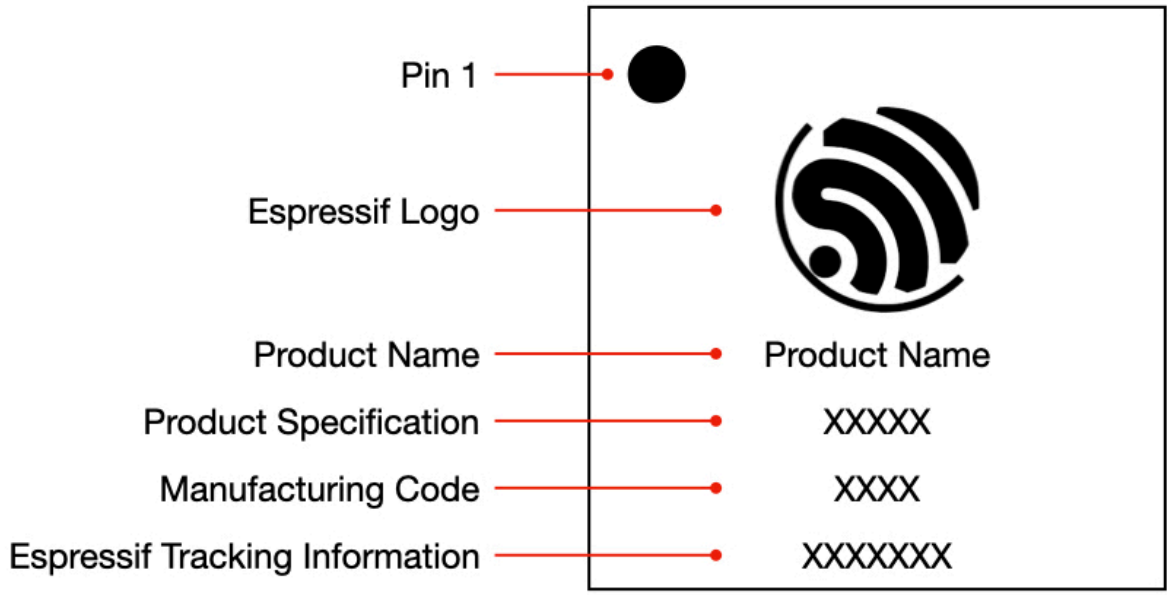

Figure 1.1: Chip Marking Diagram

Table 1.2: Chip Revision Identification by Chip Marking

Chip Revision	Manufacturing Code
v0.0	X A XX
v0.1	X B XX
v1.0	X C XX
v1.2	X D XX

Module Marking

- **Specification Identifier** line in module marking

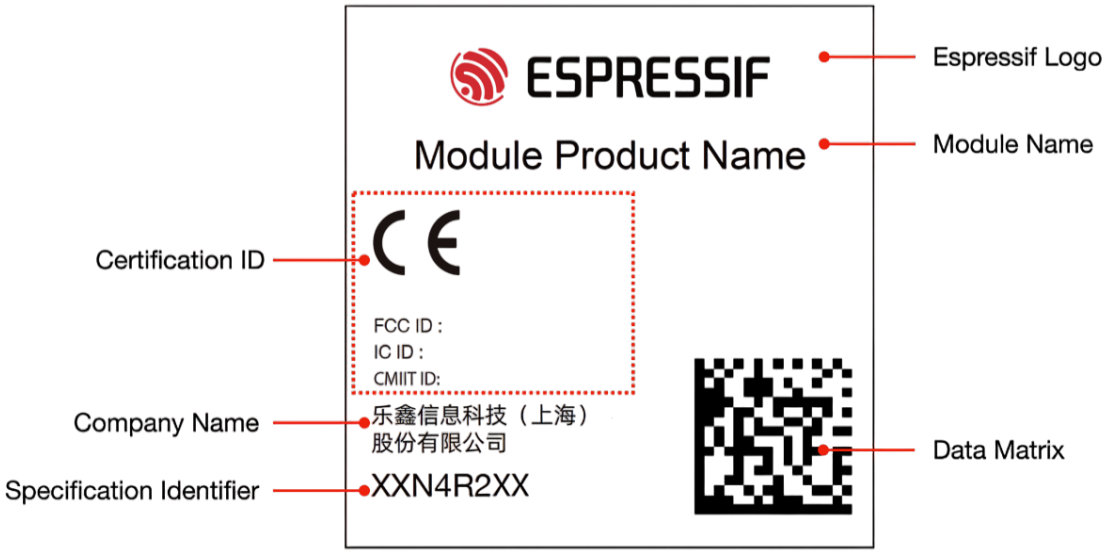

Figure 1.2: Module Marking Diagram

Table 1.3: Chip Revision Identification by Module Marking

Chip Revision	Specification Identifier
v0.0	XA XXXX
v0.1	MB XXXX
v1.0	MC XXXX
v1.2	MD XXXX

1.3 Additional Identification Methods

Date Code

Some errors in the chip product don’ t need to be fixed at the silicon level, or in other words in a new chip revision.

In this case, the chip may be identified by **Date Code** in chip marking (see *Chip Marking*). For more information, please refer to ESP32-C5 Chip Packaging Information > Chip Silk Marking.

PW Number

Modules built around the chip may be identified by **PW Number** in product label (see *Module Product Label*). For more information, please refer to ESP32-C5 Module Packaging Information > Pizza Box.

Figure 1.3: Module Product Label

Note: Please note that **PW Number** is only provided for reels packaged in aluminum moisture barrier bags (MBB).

1.4 ESP-IDF Release Compatibility

Information about ESP-IDF release that supports a specific chip revision is provided in Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.

1.5 Related Documents

- For more information about the chip revision upgrade and their identification of series products, please refer to ESP32-C5 Product/Process Change Notifications (PCN).
- For more information about the chip revision numbering scheme, see Compatibility Advisory for Chip Revision Numbering Scheme.

2 Errata Summary

Table 2.1: Errata summary

Category	Errata No.	Descriptions	Affected Revisions			
			v0.0	v0.1	v1.0	v1.2
RISC-V CPU	CPU-718	*[CPU-718] PSRAM Read-After-Write Consistency*	Y	Y	Y	
SRAM	SRAM-436	*[SRAM-436] Internal SRAM Contents May Be Corrupted After Digital Peripheral Power Domain Power-Down*			Y	
HUK	HUK-576	*[HUK-576] HUK Is Unavailable*	Y	Y	Y	
FLASH	FLASH-938	*[FLASH-938] Flash Manual Encryption May Fail When CPU Runs at 240 MHz*			Y	Y
ECC|ECDSA	ECC-833	*[ECC-833] Forcing ECC Memory Power-Down Bypasses ECDSA_DS Signature Verification*			Y	Y

3 All Errata Descriptions

3.1 [CPU-718] PSRAM Read-After-Write Consistency

Affected revisions: v0.0 v0.1 v1.0

Description

When the CPU performs random read or write accesses to PSRAM through CACHE or DMA, and one of the following conditions is true:

- PSRAM encryption or decryption is enabled, or

- When accessing PSRAM via DMA, AHB_DMA_OUT_DATA_BURST_MODE_SEL_CHn is set to 0 or 1.

Data-consistency issues may occur for CPU accesses to PSRAM.

Cause The MSPI hardware handles CPU read or write requests to PSRAM and uses an internal buffer or cache. Because of this buffering (and encryption or decryption latency), CPU read or write requests received by MSPI are not always executed on the SPI bus immediately.

If the CPU performs a write to a PSRAM address and then quickly issues a read to the same physical address, the write may still be delayed inside MSPI. In that case, MSPI can execute the read before the earlier write has actually completed on the PSRAM, leading to stale or inconsistent data being returned.

Examples

- If CACHE reads from an encrypted or decrypted PSRAM region and a cache miss occurs, the data written back can be inconsistent.
- After a DMA write to PSRAM completes, a subsequent DMA read or CACHE read of the same PSRAM region may return inconsistent data.

Workarounds

- For consistency problems caused by cache misses during encryption or decryption: Avoid enabling PSRAM encryption in workloads that perform random read or write access.
- For consistency problems when the CPU accesses PSRAM via DMA: Insert a short delay after the DMA write finishes, or before the CPU reads the same physical address, to ensure MSPI has completed the actual PSRAM write.

Solution

Fixed in chip revision v1.2.

3.2 [SRAM-436] Internal SRAM Contents May Be Corrupted After Digital Peripheral Power Domain Power-Down

Affected revisions: v1.0

Description

On some ESP32-C5 v1.0 chips, when the power-down feature of the digital peripheral power domain is enabled, part of the internal SRAM contents may be corrupted. This may trigger a CPU_LOCKUP reset or cause the system to hang.

Workaround

Starting from ESP-IDF v5.5, the power-down feature of the digital peripheral power domain is disabled for ESP32-C5 v1.0 chips.

Solution

Fixed in hardware starting from chip revision v1.2.

3.3 [HUK-576] HUK Is Unavailable

Affected revisions: v0.0 v0.1 v1.0

Description

On ESP32-C5 chips, inrush current during power-on can cause the first HUK recovery attempt to fail with a certain probability.

In the affected chip revisions, the ROM uses the HUK data immediately after power-on to derive flash encryption and decryption keys through the key manager (introduced in ESP-IDF v5.5.2). When HUK recovery fails, the ROM may fail to derive these keys.

Workaround

No workaround.

Solution

Fixed in chip revision v1.2.

The updated ROM re-powers the HUK and retries recovery if the initial attempt fails.

3.4 [FLASH-938] Flash Manual Encryption May Fail When CPU Runs at 240 MHz

Affected revisions: v1.0 v1.2

Description

On ESP32-C5 chips, flash manual encryption may fail when the CPU frequency is set to 240 MHz due to internal power consumption fluctuations.

Workaround

When performing flash manual encryption, configure the CPU frequency to 160 MHz or lower.

Solution

No fix scheduled.

3.5 [ECC-833] Forcing ECC Memory Power-Down Bypasses ECDSA_DS Signature Verification

Affected revisions: v1.0 v1.2

Description

On ESP32-C5 chips, if ECC memory is force-powered down via the system register, ECDSA_DS reports any submitted signature as valid.

Workaround

Use RSA_DS instead of ECDSA_DS for signature verification.

Solution

To be fixed in the next chip revision.

4 Revision History

Table 4.1: Revision History

Date	Version	Release Notes
2026-06-12	v1.2	*All Errata Descriptions* • Added Section *[ECC-833] Forcing ECC Memory Power-Down Bypasses ECDSA_DS Signature Verification*
2026-03-04	v1.1	·*Chip Revision Identification* – Added information about chip revision v1.2 ·*All Errata Descriptions* – In Section *[CPU-718] PSRAM Read-After-Write Consistency*, updated solution to "fixed in chip revision v1.2" – Added Section *[SRAM-436] Internal SRAM Contents May Be Corrupted After Digital Peripheral Power Domain Power-Down* – Added Section *[HUK-576] HUK Is Unavailable* – Added Section *[FLASH-938] Flash Manual Encryption May Fail When CPU Runs at 240 MHz*
2025-11-05	v1.0	First release

5 Related Documentation and Resources

5.1 Related Documentation

- ESP32-C5 Datasheet –Specifications of the ESP32-C5 hardware.
- ESP32-C5 Technical Reference Manual –Detailed information on how to use the ESP32-C5 memory and peripherals.
- ESP32-C5 Hardware Design Guidelines –Guidelines on how to integrate the ESP32-C5 into your hardware product.
- Certificates
  https://espressif.com/en/support/documents/certificates
- ESP32-C5 Product/Process Change Notifications (PCN)
  https://espressif.com/en/support/documents/pcns?keys=ESP32-C5
- ESP32-C5 Advisories –Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-C5
- Documentation Updates and Update Notification Subscription
  https://espressif.com/en/support/download/documents

5.2 Developer Zone

- ESP-IDF Programming Guide for ESP32-C5 –Extensive documentation for the ESP-IDF development framework.
- ESP-IDF and other development frameworks on GitHub.
  https://github.com/espressif
- ESP32 BBS Forum –Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- The ESP Journal –Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs SDKs and Demos, Apps, Tools, AT Firmware.
  https://espressif.com/en/support/download/sdks-demos

5.3 Products

- ESP32-C5 Series SoCs –Browse through all ESP32-C5 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C5
- ESP32-C5 Series Modules –Browse through all ESP32-C5-based modules.
  https://espressif.com/en/products/modules?id=ESP32-C5
- ESP32-C5 Series DevKits –Browse through all ESP32-C5-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-C5
- ESP Product Selector –Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector

5.4 Contact Us

- See the tabs Sales Questions, Technical Enquiries, Circuit Schematic & PCB Design Review, Get Samples (Online stores), Become Our Supplier, Comments & Suggestions.
  https://espressif.com/en/contact-us/sales-questions

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