ESP32-H2

Series SoC Errata Version 0.5

ESPRESSIF

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1 Chip Revision Identification

Espressif is introducing a new **vM.X** numbering scheme to indicate chip revisions. This guide outlines the structure of this scheme and provides information on chip errata and additional identification methods.

1.1 Chip Revision Numbering Scheme

The new numbering scheme **vM.X** consists of the major and minor numbers described below.

M –Major number, indicating the major revision of the chip product. If this number changes, it means the software used for the previous version of the product is incompatible with the new product, and the software version shall be upgraded for the use of the new product.

X –Minor number, indicating the minor revision of the chip product. If this number changes, it means the software used for the previous version of the product is compatible with the new product, and there is no need to upgrade the software.

The **vM.X** scheme replaces previously used chip revision schemes, including ECOx numbers, Vxxx, and other formats if any.

1.2 Primary Identification Methods

eFuse Bits

The chip revision is encoded using two eFuse fields:

- EFUSE_RD_MAC_SYS_3_REG[22:21]
- EFUSE_RD_MAC_SYS_3_REG[20:18]

Table 1.1: Chip Revision Identification by eFuse Bits

	eFuse Bit	Chip Revision	
		v0.0	v0.1
Major Number	EFUSE_RD_MAC_SYS_3_REG[22]	0	0
	EFUSE_RD_MAC_SYS_3_REG[21]	0	0
Minor Number	EFUSE_RD_MAC_SYS_3_REG[20]	0	0
	EFUSE_RD_MAC_SYS_3_REG[19]	0	0
	EFUSE_RD_MAC_SYS_3_REG[18]	0	1

Chip Marking

- **Espressif Tracking Information** line in chip marking

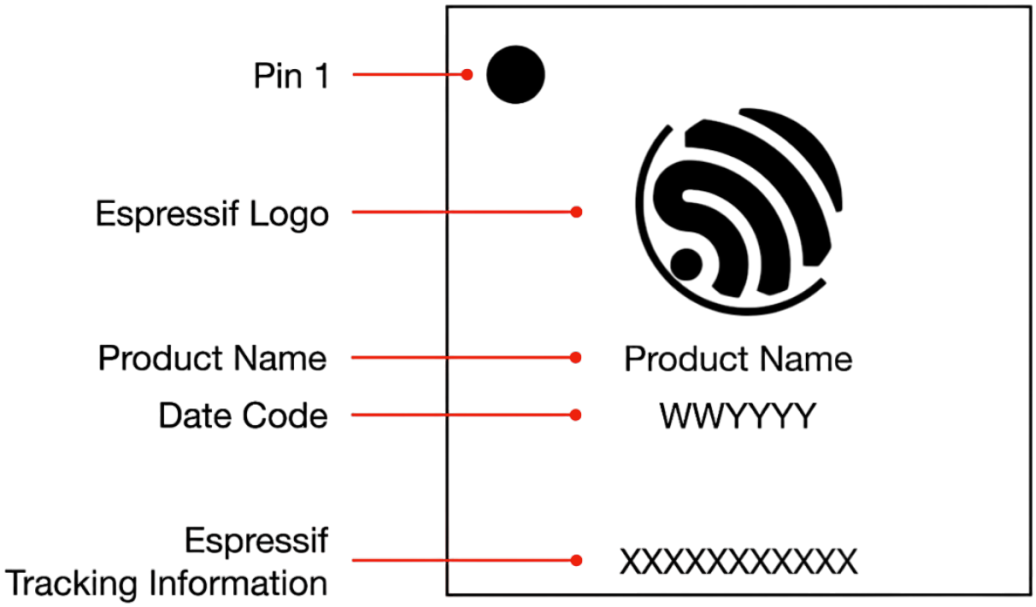

Figure 1.1: Chip Marking Diagram

Table 1.2: Chip Revision Identification by Chip Marking

Chip Revision	Espressif Tracking Information
v0.0	X A XXXXXXXX
v0.1	X B XXXXXXXX

Module Marking

- **Specification Identifier** line in module marking

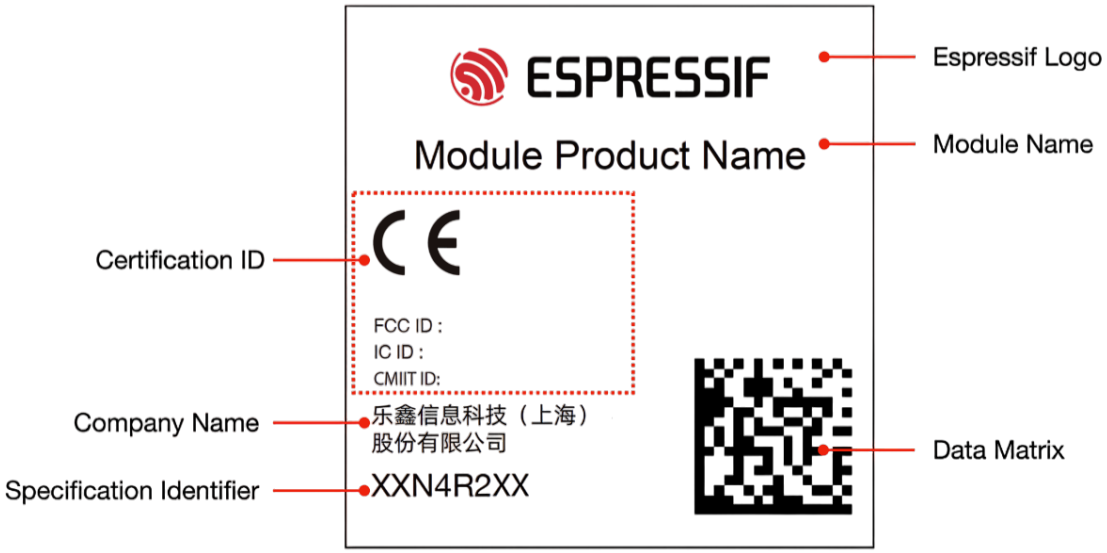

Figure 1.2: Module Marking Diagram

Table 1.3: Chip Revision Identification by Module Marking

Chip Revision	Specification Identifier
v0.0	—[1]
v0.1	MB XXXX

[1] Missing specification identifier "—" means modules with this chip revision are not mass produced.

1.3 Additional Identification Methods

Date Code

Some errors in the chip product don't need to be fixed at the silicon level, or in other words in a new chip revision.

In this case, the chip may be identified by **Date Code** in chip marking (see *Chip Marking Diagram*). For more information, please refer to Espressif Chip Packaging Information.

PW Number

Modules built around the chip may be identified by **PW Number** in product label (see *Module Product Label*). For more information, please refer to Espressif Module Packaging Information.

Figure 1.3: Module Product Label

Note: Please note that **PW Number** is only provided for reels packaged in aluminum moisture barrier bags (MBB).

1.4 ESP-IDF Release Compatibility

Information about ESP-IDF release that supports a specific chip revision is provided in Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.

1.5 Related Documents

- For more information about the chip revision upgrade and their identification of series products, please refer to ESP32-H2 Product/Process Change Notifications (PCN).
- For more information about the chip revision numbering scheme, see Compatibility Advisory for Chip Revision Numbering Scheme.

2 Errata Summary

Table 2.1: Errata summary

Category	Descriptions	Affected Revisions	
		v0.0	v0.1
RISC-V CPU	*[CPU] Possible Deadlock Due to Out-of-Order Execution of Instructions When Writing to LP SRAM Is Involved*	Y	Y
Clock	*[Clock] Inaccurate Calibration of RC_FAST_CLK Clock*	Y	Y
SAR ADC	*[SAR ADC] Unavailable Channel 4 in SRA ADC1*	Y	Y

3 All Errata Descriptions

3.1 [CPU] Possible Deadlock Due to Out-of-Order Execution of Instructions When Writing to LP SRAM Is Involved

Affected revisions: v0.0 v0.1

Description

When HP CPU executes instructions (instruction A and instruction B successively) in LP SRAM, and instruction A and instruction B happen to follow the following patterns:

- Instruction A involves writing to memory. Examples: **sw/sh/sb**
- Instruction B involves only accessing the instruction bus. Examples: **nop/jal/jalr/lui/auipc**
- The address of instruction B is not 4-byte aligned

The data written by instruction A to memory is only committed after instruction B has completed execution. This introduces a risk where, after instruction A writing to memory, if an infinite loop is executed in instruction B, the writing of instruction A will never complete.

Workarounds

When you experience this problem, or when you check the assembly code and see the above mentioned pattern,

- Add a **fence** instruction between instruction A and the infinite loop. This can be achieved by using the *rv_utils_memory_barrier* interface in ESP-IDF.
- Replace the infinite loop with instruction **wfi**. This can be achieved by using the *rv_utils_wait_for_intr* interface in ESP-IDF.
- Disable the RV32C (compressed) extension when compiling code that to be executed in LP SRAM to avoid instructions with not 4-byte aligned addresses.

Solution

To be fixed in the future chip revisions.

3.2 [Clock] Inaccurate Calibration of RC_FAST_CLK Clock

Affected revisions: v0.0 v0.1

Description

In the ESP32-H2 chip, the frequency of the RC_FAST_CLK clock source is too close to the reference clock (32 MHz XTAL_CLK) frequency, making it impossible to calibrate accurately. This may affect peripherals that use RC_FAST_CLK and have stringent requirements for its accurate clock frequency.

For peripherals using RC_FAST_CLK, please refer to *ESP32-H2 Technical Reference Manual* > *Chapter Reset and Clock* [PDF].

Workarounds

Use other clock sources instead of RC_FAST_CLK.

Solution

To be fixed in the next chip revision.

3.3 [SAR ADC] Unavailable Channel 4 in SRA ADC1

Affected revisions: v0.0 v0.1

Description

Channel 4 (ADC1_CH4) of ADC1 is not operational in the ESP32-H2 chip.

Workarounds

Use other channels instead of ADC1_CH4.

Solution

To be fixed in the next chip revision.

4 Revision History

Table 4.1: Revision History

Date	Version	Release Notes
2023-10-17	v0.5	First release

5 Related Documentation and Resources

5.1 Related Documentation

- ESP32-H2 Datasheet –Specifications of the ESP32-H2 hardware.
- ESP32-H2 Technical Reference Manual –Detailed information on how to use the ESP32-H2 memory and peripherals.
- ESP32-H2 Hardware Design Guidelines –Guidelines on how to integrate the ESP32-H2 into your hardware product.
- Certificates
  https://espressif.com/en/support/documents/certificates
- ESP32-H2 Product/Process Change Notifications (PCN)
  https://espressif.com/en/support/documents/pcns?keys=ESP32-H2
- ESP32-H2 Advisories –Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-H2
- Documentation Updates and Update Notification Subscription
  https://espressif.com/en/support/download/documents

5.2 Developer Zone

- ESP-IDF Programming Guide for ESP32-H2 –Extensive documentation for the ESP-IDF development framework.

- ESP-IDF and other development frameworks on GitHub.
  https://github.com/espressif
- ESP32 BBS Forum –Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- The ESP Journal –Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs SDKs and Demos, Apps, Tools, AT Firmware.
  https://espressif.com/en/support/download/sdks-demos

5.3 Products

- ESP32-H2 Series SoCs –Browse through all ESP32-H2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-H2
- ESP32-H2 Series Modules –Browse through all ESP32-H2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-H2
- ESP32-H2 Series DevKits –Browse through all ESP32-H2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-H2
- ESP Product Selector –Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector

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