ESP32-C2

Hardware Design Guidelines

Release master
Espressif Systems
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Table of contents

This document provides guidelines for the ESP32-C2 SoC.

Important: The ESP32-C2 SoC currently consists of only one series, the ESP8684, so the references of ESP32-C2 in this document refers to the ESP8684 Series SoCs.

		
Schematic Checklist	PCB Layout Design	Hardware Development

Chapter 1

About This Document

1.1 Introduction

The hardware design guidelines advise on how to integrate ESP32-C2 into a product. These guidelines will help to achieve optimal performance of your product, ensuring technical accuracy and adherence to Espressif's standards. The guidelines are intended for hardware and application engineers.

The document assumes that you possess a certain level of familiarity with the ESP32-C2 SoC. In case you lack prior knowledge, we recommend utilizing this document in conjunction with the ESP32-C2 Series Datasheet.

1.2 Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32c2/index.html

Chapter 2

Product Overview

ESP32-C2 is a system on a chip that integrates the following features:

- Wi-Fi (2.4 GHz band)
- Bluetooth® 5 (LE)
- High-performance 32-bit RISC-V single-core processor
- Multiple peripherals
- Intended for simple, high-volume IoT applications

Powered by 40 nm technology, ESP32-C2 provides a robust, highly-integrated platform, which helps meet the continuous demands for efficient power usage, compact design, security, high performance, and reliability. Typical application scenarios for ESP32-C2 include:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

For more information about ESP32-C2, please refer to ESP32-C2 Series Datasheet.

Note: Unless otherwise specified, "ESP32-C2" used in this document refers to the series of chips, instead of a specific chip variant.

Chapter 3

Schematic Checklist

The integrated circuitry of ESP32-C2 requires only 15 electrical components (resistors, capacitors, and inductors) and a crystal. The high integration of ESP32-C2 allows for simple peripheral circuit design. This chapter details the schematic design of ESP32-C2.

The following figure shows a reference schematic design of ESP32-C2. It can be used as the basis of your schematic design.

Important: Starting from chip revision v1.1, the ESP32-C2 firmware supports both 26 MHz and 40 MHz crystals. For ESP32-C2 revision v1.0 and previous chips, please use 26 MHz instead of 40 MHz crystal. For details, you can refer to ESP32-C2 Series SoC Errata (PDF). You can also contact the sales team to check the chip revision.

Any basic ESP32-C2 circuit design may be broken down into the following major building blocks:

- *Power supply*
- *Chip power-up and reset timing*
- *Flash*
- *Clock source*
- *RF*
- *UART*
- *Strapping pins*
- *GPIO*
- *ADC*

The rest of this chapter details the specifics of circuit design for each of these sections.

3.1 Power Supply

The general recommendations for power supply design are:

- When using a single power supply, the recommended power supply voltage is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add an ESD protection diode at the power entrance.

More information about power supply pins can be found in ESP32-C2 Series Datasheet > Section *Power Supply*.

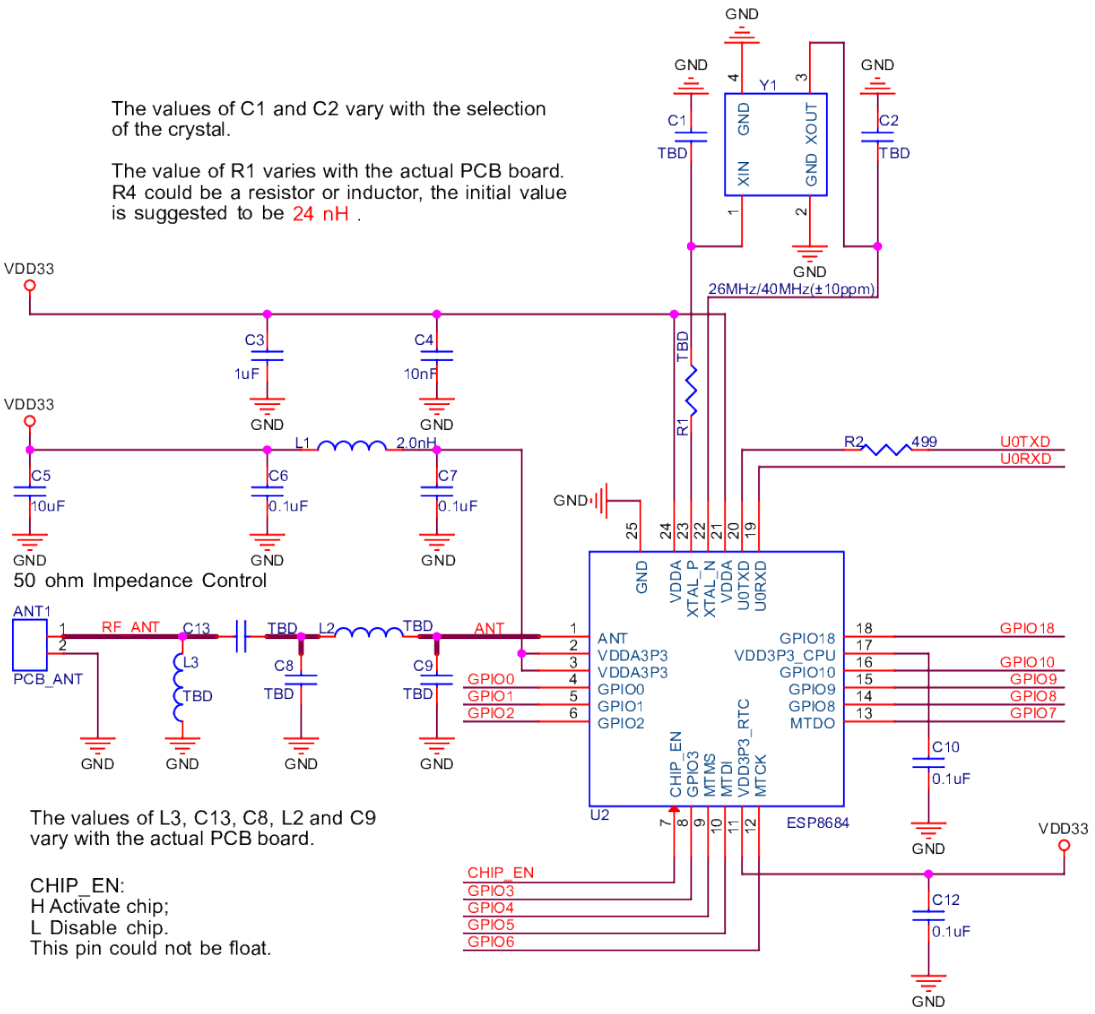

Fig. 1: ESP32-C2 Reference Schematic

3.1.1 Digital Power Supply

ESP32-C2 has pin17 VDD3P3_CPU as the digital power supply pin(s) working in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 µF decoupling capacitor close to the pin(s).

The schematic for the digital power supply pins is shown in Figure *ESP32-C2 Schematic for Digital Power Supply Pins*.

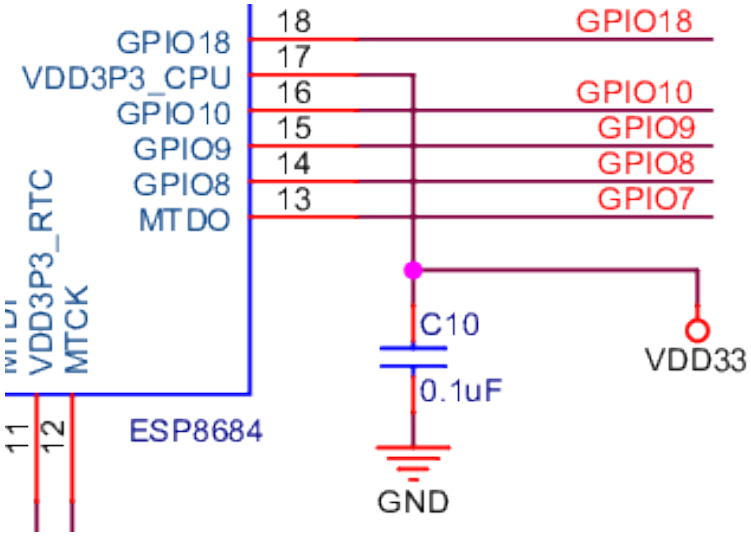

Fig. 2: ESP32-C2 Schematic for Digital Power Supply Pins

3.1.2 Analog Power Supply

ESP32-C2's VDDA and VDDA3P3 pins are the analog power supply pins, working at 3.0 V ~ 3.6 V.

For VDDA3P3, when ESP32-C2 is transmitting signals, there may be a sudden increase in the current draw, causing power rail collapse. Therefore, it is highly recommended to add a 10 µF capacitor to the power rail, which can work in conjunction with the 0.1 µF capacitor(s).

It is suggested to add an extra 10 µF capacitor at the power entrance. If the power entrance is close to VDDA3P3, then two 10 µF capacitors can be merged into one.

Add a LC circuit on the VDDA3P3 power rail to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA and above.

Place appropriate decoupling capacitors near the other analog power pins according to Figure *ESP32-C2 Schematic for Analog Power Supply Pins*.

If a two-layer board design is used, it is recommended to change the CLC filter circuit for VDDA3P3 to a CCL structure, as placing the inductance closer to the chip will yield better performance. Please refer to Figure *ESP32-C2 Schematic for Analog Power Supply Pins (Two-layer Board)* for details.

3.1.3 RTC Power Supply

ESP32-C2's VDD3P3_RTC pin is the RTC and analog power pin. It is recommended to place a 0.1 µF decoupling capacitor near this power pin in the circuit.

Note that this power supply cannot be used as a single backup power supply.

The schematic for the RTC power supply pin is shown in Figure *ESP32-C2 Schematic for RTC Power Supply Pin*.

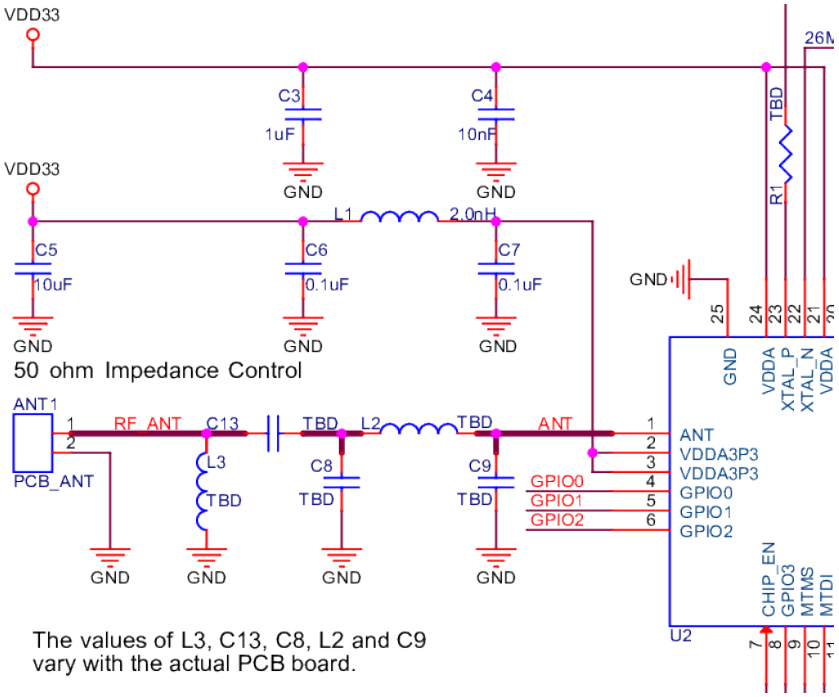

Fig. 3: ESP32-C2 Schematic for Analog Power Supply Pins

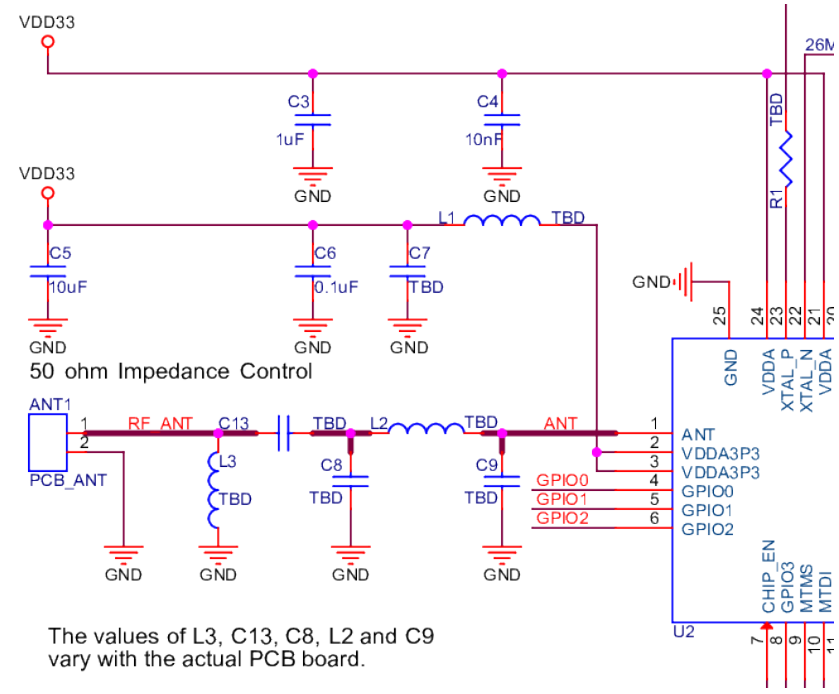

Fig. 4: ESP32-C2 Schematic for Analog Power Supply Pins (Two-layer Board)

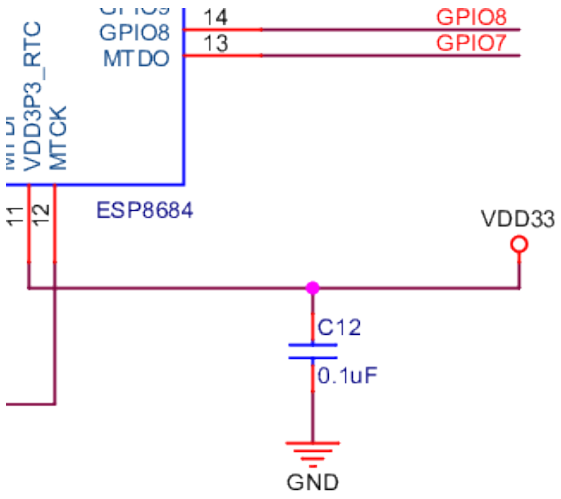

Fig. 5: ESP32-C2 Schematic for RTC Power Supply Pin

3.2 Chip Power-up and Reset Timing

ESP32-C2 ' s CHIP_EN pin can enable the chip when it is high and reset the chip when it is low.

When ESP32-C2 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_EN is pulled up and the chip is enabled. Therefore, CHIP_EN needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage V_{IL_nRST} in the range of (–0.3 ~ 0.25 × VDD) V. To avoid reboots caused by external interferences, make the CHIP_EN trace as short as possible.

Figure *ESP32-C2 Power-up and Reset Timing* shows the power-up and reset timing of ESP32-C2.

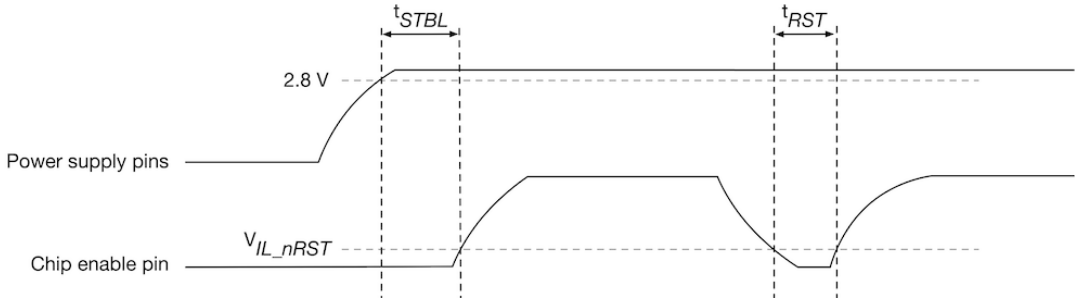

Fig. 6: ESP32-C2 Power-up and Reset Timing

Table *Description of Timing Parameters for Power-up and Reset* provides the specific timing requirements.

Table 1: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Minimum (µs)
t_{STBL}	Time reserved for the power rails to stabilize before the CHIP_EN pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_EN to stay below V_{IL_nRST} to reset the chip	50

Attention:

- CHIP_EN must not be left floating.

- To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP_EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 µF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.
- If the user application has one of the following scenarios:
  - Slow power rise or fall, such as during battery charging.
  - Frequent power on/off operations.
  - Unstable power supply, such as in photovoltaic power generation.

  Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:
  - Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
  - Implementing reset functionality through a button or the main controller.

3.3 Flash

ESP32-C2 series of chips have in-package 1 MB, 2 MB or 4 MB flash. The pins for flash are not bonded out.

3.4 Clock Source

ESP32-C2 supports two external clock sources:

- *External crystal clock source (Compulsory)*
- *RTC clock source (Optional)*

3.4.1 External Crystal Clock Source (Compulsory)

Important: Starting from chip revision v1.1, the ESP32-C2 firmware supports both 26 MHz and 40 MHz crystals. For ESP32-C2 revision v1.0 and previous chips, please use 26 MHz instead of 40 MHz crystal. For details, you can refer to ESP32-C2 Series SoC Errata (PDF). You can also contact the sales team to check the chip revision.

The circuit for the crystal is shown in Figure *ESP32-C2 Schematic for External Crystal*. Note that the accuracy of the selected crystal should be within ±10 ppm.

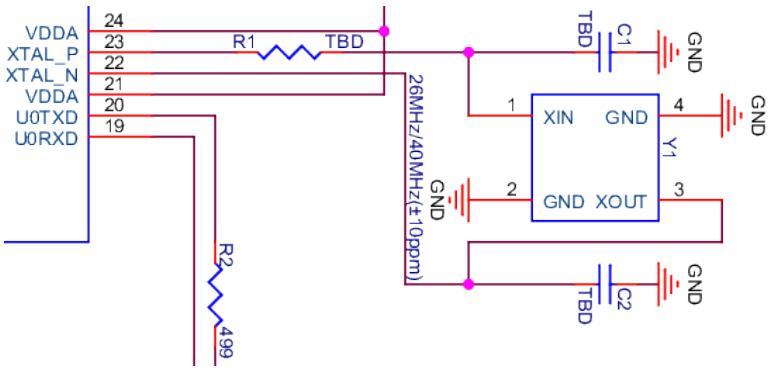

Fig. 7: ESP32-C2 Schematic for External Crystal

Please add a series component (resistor or inductor) on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C2 can be determined according to the formula:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C2 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.
2. Observe the 2.4 GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.

- When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
- When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
- External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

Note:

- Defects in the manufacturing of crystal (for example, large frequency deviation of more than ±10 ppm, unstable performance within the operating temperature range, etc) may lead to the malfunction of ESP32-C2, resulting in a decrease of the RF performance.
- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

3.4.2 RTC Clock Source (Optional)

ESP32-C2 supports an external 32.768 kHz crystal or an external signal (e.g., an oscillator) to act as the RTC clock. The external RTC clock source enhances timing accuracy and consequently decreases average power consumption, without impacting functionality.

If the RTC clock source is not required, then the pins for the 32.768 kHz crystal can be used as GPIOs.

3.5 RF

3.5.1 RF Circuit

ESP32-C2's RF circuit is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit. Each part should meet the following requirements:

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. A CLCCL structure is preferred.
  - The CLCCL structure forms a bandpass filter, which is mainly used to adjust impedance points, suppress harmonics, and suppress low-frequency noise (especially in applications such as electrical lighting where the effect is significant). If there is no AC-to-DC circuit in the user application, a simpler CLC structure can be considered.
  - The RF matching circuit is shown in Figure *ESP32-C2 Schematic for RF Matching*.
- For the antenna and the antenna matching circuit, to ensure radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

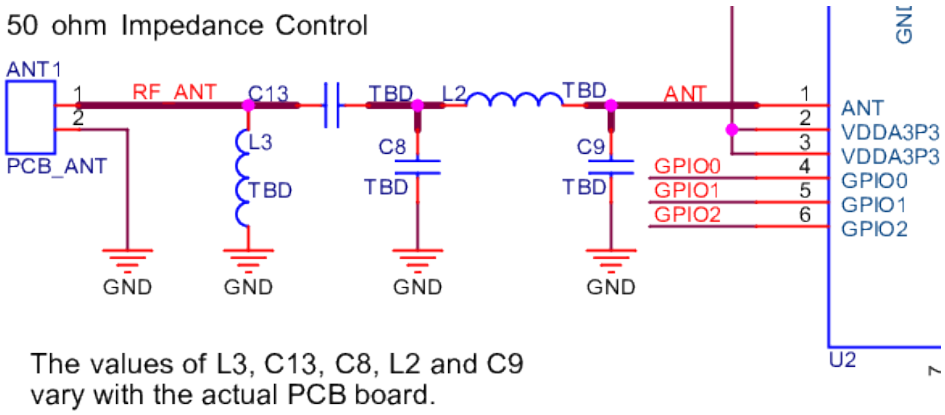

Fig. 8: ESP32-C2 Schematic for RF Matching

3.5.2 RF Tuning

The RF matching parameters vary with the board, so the ones used in Espressif modules could not be applied directly. Follow the instructions below to do RF tuning.

Figure *ESP32-C2 RF Tuning Diagram* shows the general process of RF tuning.

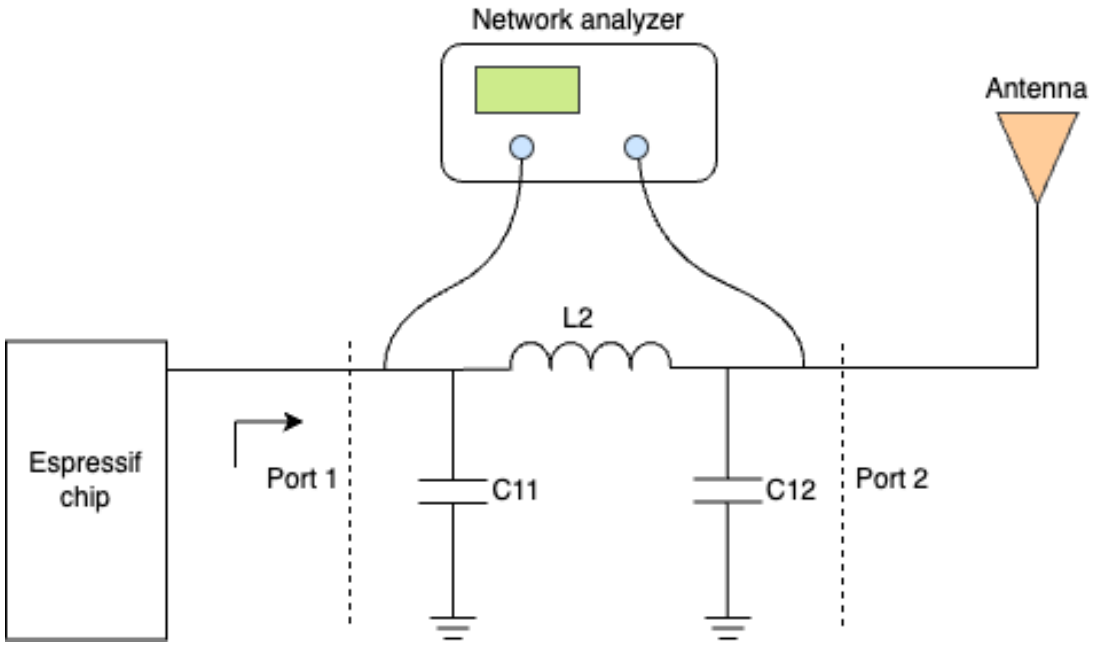

Fig. 9: ESP32-C2 RF Tuning Diagram

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, the transmission performance is best if the matching impedance is conjugate to the chip impedance. S21 is used to describe the transmission loss of signal from Port 1 to Port 2. If S11 is close to the chip conjugate point (30+j0) and S21 is less than -35 dB at 4.8 GHz and 7.2 GHz, the matching circuit can satisfy transmission requirements.

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter *PCB Layout Design*, you can refer to the value ranges in Table *Recommended Value Ranges for Components* to debug the matching circuit.

Table 2: Recommended Value Ranges for Components

Reference Designator	Recommended Value Range	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.4 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

If the components are in the 0201 SMD package size, please use a stub in the PCB design of the RF matching circuit near the chip. If the antenna input impedance is not 50 ohm, an additional set of RF matching is recommended for antenna tuning.

If the usage or production environment is sensitive to electrostatic discharge, it is recommended to reserve ESD protection devices near the antenna.

Note: If RF function is not required, then the RF pin can be left floating.

3.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line to suppress the 80 MHz harmonics.

Usually, UART0 is used as the serial port for download and log printing. For instructions on download over UART0, please refer to Section *Download Guidelines*.

Other UART interfaces can be used as serial ports for communication, which could be mapped to any available GPIO by software configurations. For these interfaces, it is also recommended to add a series resistor to the TX line to suppress harmonics.

When using the AT firmware, please note that the UART GPIO is already configured (refer to AT Firmware Download). It is recommended to use the default configuration.

3.7 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

All the information about strapping pins is covered in ESP32-C2 Series Datasheet > Section *Strapping Pins*. In this document, we will mainly cover the strapping pins related to boot mode.

After chip reset is released, the combination of GPIO8 and GPIO9 controls the boot mode. See Table *Boot Mode Control*.

Table 3: Boot Mode Control

Boot Mode	GPIO8	GPIO9
Default Config	–(Floating)	1 (Pull-up)
SPI Boot (default)	Any value	1
Joint Download Boot[1]	1	0
Invalid combination[2]	0	0

Signals applied to the strapping pins should have specific *setup time* and *hold time*. For more information, see Figure *Setup and Hold Times for Strapping Pins* and Table *Description of Timing Parameters for Strapping Pins*.

[1] Joint Download Boot mode supports UART Download Boot download method. In addition to SPI Boot and Joint Download Boot modes, ESP32-C2 also supports SPI Download Boot mode. For details, please see ESP32-C2 Technical Reference Manual > Chapter *Chip Boot Control*.

[2] This combination triggers unexpected behavior and should be avoided.

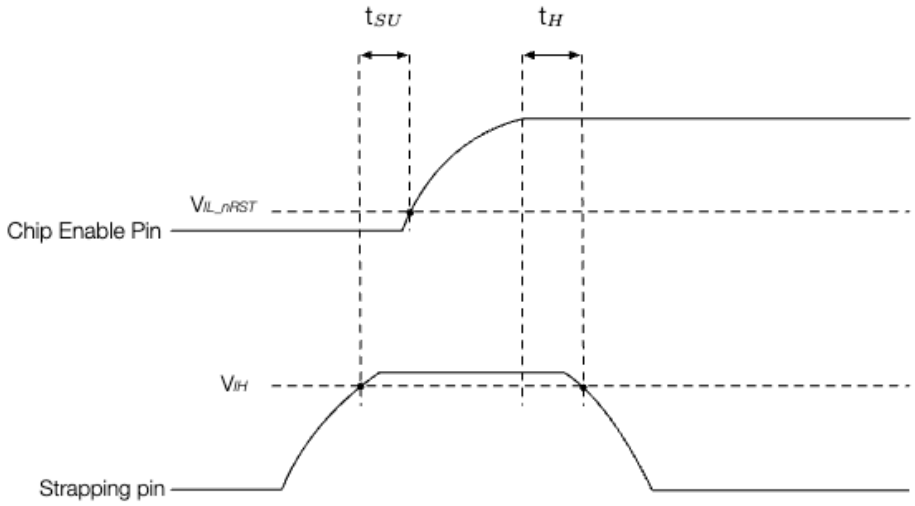

Fig. 10: Setup and Hold Times for Strapping Pins

Table 4: Description of Timing Parameters for Strapping Pins

Parameter	Description	Minimum (ms)
t_{SU}	Time reserved for the power rails to stabilize before the chip enable pin (CHIP_EN) is pulled high to activate the chip.	0
t_H	Time reserved for the chip to read the strapping pin values after CHIP_EN is already high and before these pins start operating as regular IO pins.	3

Attention: Do not add high-value capacitors at GPIO9, otherwise, the chip may not boot successfully.

3.8 GPIO

The pins of ESP32-C2 can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations, whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to ESP32-C2 Technical Reference Manual > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals have already been routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to ESP32-C2 Series Datasheet > Section *Peripheral Pin Configurations*.

When using GPIOs, please:

- Pay attention to the states of strapping pins during power-up.
- Pay attention to the default configurations of the GPIOs after reset. The default configurations can be found in Table *IO MUX Pin Functions*. It is recommended to add a pull-up or pull-down resistor to pins in the high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.
- Some pins will have glitches during power-up. Refer to Table *Power-Up Glitches on Pins* for details.

Table 5: IO MUX Pin Functions

Pin Name	No.	Function 0	Function 1	Function 2	Reset	Notes
GPIO0	4	GPIO0	GPIO0	—	0	R, G
GPIO1	5	GPIO1	GPIO1	—	0	R, G
GPIO2	6	GPIO2	GPIO2	FSPIQ	1	R
GPIO3	8	GPIO3	GPIO3	—	1	R, G
MTMS	9	MTMS	GPIO4	FSPIHD	1	R
MTDI	10	MTDI	GPIO5	FSPIWP	1	R, G
MTCK	12	MTCK	GPIO6	FSPICLK	1*	—
MTDO	13	MTDO	GPIO7	FSPID	1	—
GPIO8	14	GPIO8	GPIO8	—	1	—
GPIO9	15	GPIO9	GPIO9	—	3	—
GPIO10	16	GPIO10	GPIO10	FSPICS0	1	—
GPIO18	18	GPIO18	GPIO18	—	0	—
U0RXD	19	U0RXD	GPIO19	—	3	—
U0TXD	20	U0TXD	GPIO20	—	4	—

Reset:

The default configuration of each pin after reset:

- 0 –input disabled, in high impedance state (IE = 0)
- 1 –input enabled, in high impedance state (IE = 1)
- 2 –input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- 3 –input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- 4 –output enabled, pull-up resistor enabled (OE = 1, WPU = 1)
- 1* –When the value of eFuse bit EFUSE_DIS_PAD_JTAG is
  - 0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
  - 1, input enabled, in high impedance state (IE = 1)

Notes:

- R –These pins have analog functions.
- G –These pins have glitches during power-up. See details in *Power-Up Glitches on Pins*.

Table 6: Power-Up Glitches on Pins

Pin	Glitch[3]	Typical Time (µs)
GPIO0	Low-level glitch	40
GPIO1	Low-level glitch	60
GPIO3	Low-level glitch	60
MTDI	Low-level glitch	60

3.9 ADC

Please add a 0.1 µF filter capacitor between ESP pins and ground when using the ADC function to improve accuracy.

The calibrated ADC results after hardware calibration and software calibration are shown in the list below. For higher accuracy, you may implement your own calibration methods.

- When ATTEN=0 and the effective measurement range is 0 ~ 950 mV, the total error is ±5 mV.
- When ATTEN=3 and the effective measurement range is 0 ~ 2800 mV, the total error is ±10 mV.

[3] Low-level glitch: the pin is at a low level output status during the time period;

Chapter 4

PCB Layout Design

This chapter introduces the key points of how to design an ESP32-C2 PCB layout using an ESP32-C2 module (see Figure *ESP32-C2 Reference PCB Layout*) as an example.

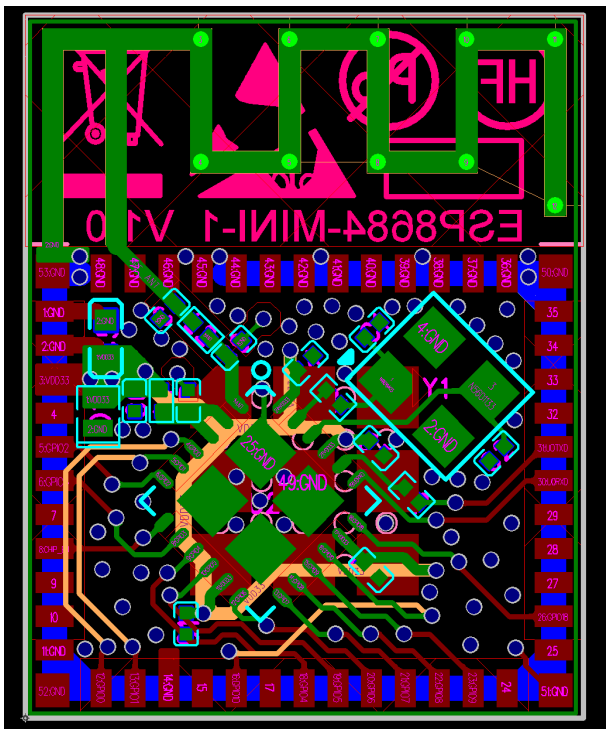

Fig. 1: ESP32-C2 Reference PCB Layout

4.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

4.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the baseboard on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

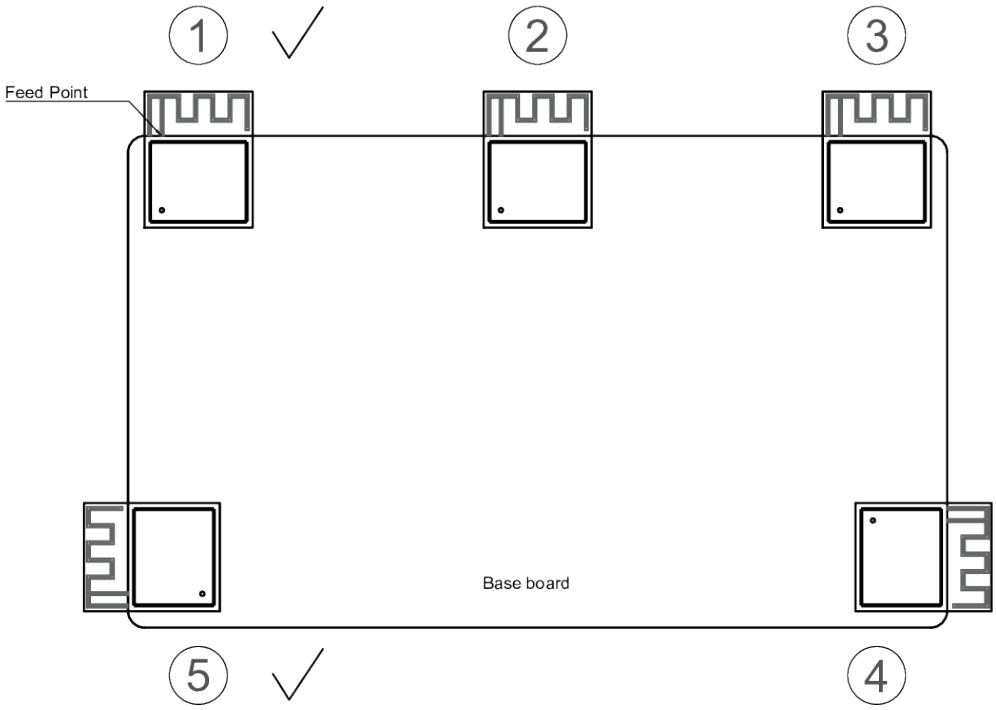

Fig. 2: Placement of ESP32-C2 Modules on Base Board (antenna feed point on the left)

If the PCB antenna cannot be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure *Keepout Zone for ESP32-C2 Module's Antenna on the Base Board* shows the suggested clearance for modules whose antenna feed point is on the left.

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification. It is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

4.3 Power Supply

Figure *ESP32-C2 Power Traces in a Four-layer PCB Design* shows the overview of the power traces in a four-layer PCB design.

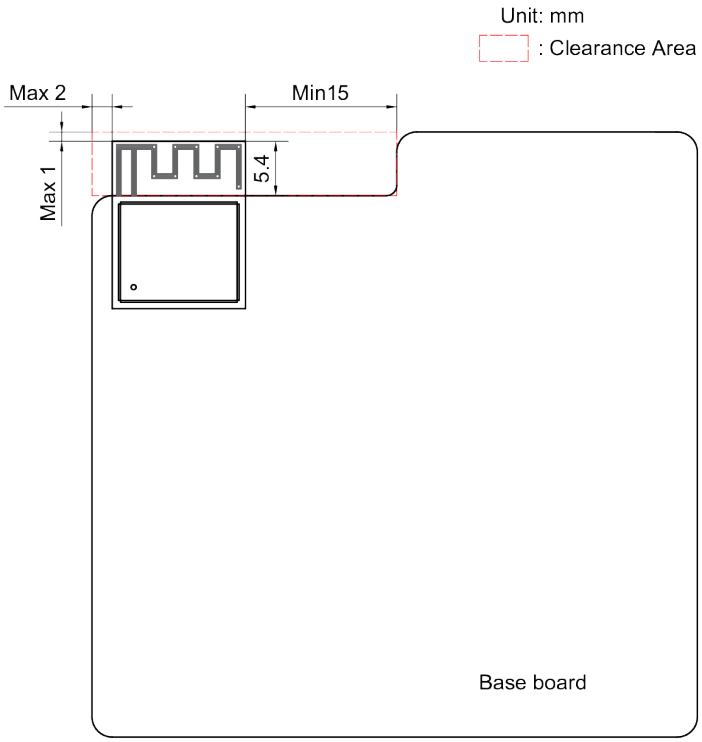

Fig. 3: Keepout Zone for ESP32-C2 Module’ s Antenna on the Base Board

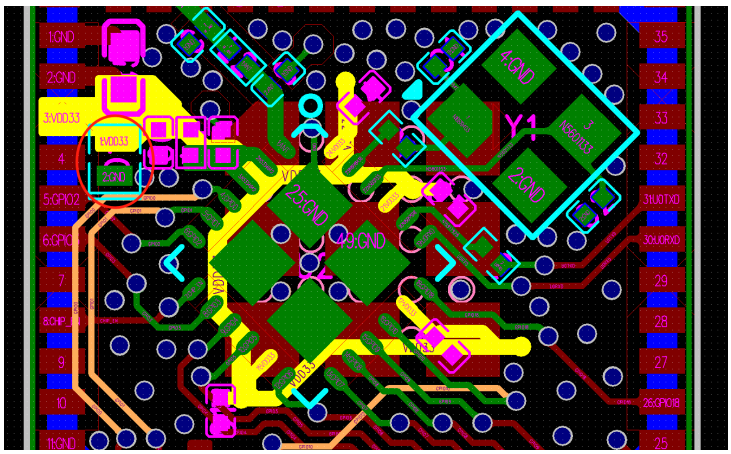

Fig. 4: ESP32-C2 Power Traces in a Four-layer PCB Design

Figure *ESP32-C2 Power Traces in a Two-layer PCB Design* shows the overview of the power traces in a two-layer PCB design.

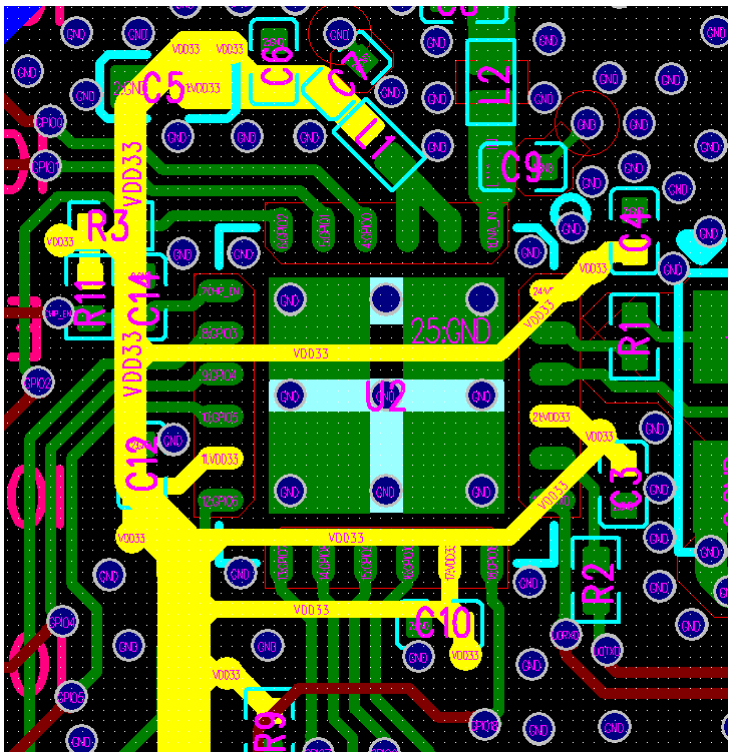

Fig. 5: ESP32-C2 Power Traces in a Two-layer PCB Design

4.3.1 General Guidelines

- Four-layer PCB design is preferred.
- The power traces should be routed on the inner third layer whenever possible.
- Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure *ESP32-C2 Power Traces in a Four-layer PCB Design*. This can avoid chip displacement caused by tin leakage and bubbles when soldering the module EPAD to the substrate.

4.3.2 3.3 V Power Layout

The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure *ESP32-C2 Power Traces in a Four-layer PCB Design*.

The 3.3 V power layout should meet the following guidelines:

- The ESD protection diode is placed next to the power port (circled in red in Figure *ESP32-C2 Power Traces in a Four-layer PCB Design*). The power trace should have a 10 µF capacitor on its way before entering into the chip, and a 0.1 or 1 µF capacitor could also be used in conjunction. After that, the power traces are divided into several branches using a star-shaped topology, which reduces the coupling between different power pins. Note that all decoupling capacitors should be placed close to the corresponding power pin, and ground vias should be added close to the capacitor’ s ground pad to ensure a short return path.

- In Figure *ESP32-C2 Power Traces in a Four-layer PCB Design*, the 10 µF capacitor is shared by the analog power supply VDDA3P3, and the power entrance since the analog power is close to the chip power entrance. If the chip power entrance is not near VDDA3P3, it is recommended to add a 10 µF capacitor to both the chip power entrance and VDDA3P3. Also, reserve two 1 µF capacitors if space permits.
- The width of the main power traces should be no less than 20 mil. The width of VDDA3P3 power traces should be no less than 15 mil. The recommended width of other power traces is 10 mil.

4.3.3 Analog Power Layout

Figure *ESP32-C2 Analog Power Traces in a Four-layer PCB Design* shows the analog power layout in a four-layer PCB design.

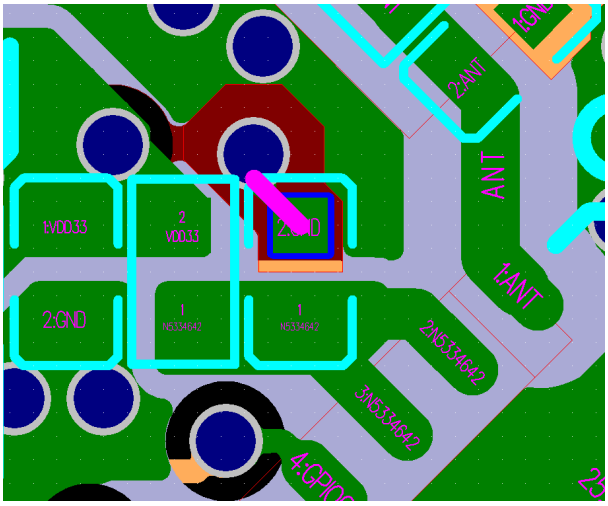

Fig. 6: ESP32-C2 Analog Power Traces in a Four-layer PCB Design

The analog power layout should meet the following guidelines:

- As shown in Figure *ESP32-C2 Analog Power Traces in a Four-layer PCB Design*, it is recommended to connect the capacitor to ground in the LC filter circuit near VDDA3P3 to the fourth layer through a via, and maintain a keep-out area on other layers. The purpose is to further reduce harmonic interference.
- VDDA3P3 analog power supply should be surrounded by ground copper. It is required to add GND isolation between VDDA3P3, power trace and the surrounding GPIO and RF traces, and place vias whenever possible.

4.4 Crystal

Figure *ESP32-C2 Crystal Layout (without Keep-out Area on Top Layer)* shows the layout for the crystal that is connected to the ground through vias but there is no keep-out area on the top layer for ground isolation.

The layout of the crystal should follow the guidelines below:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 2.0 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers. The clock traces should not intersect with each other.
- Components in series to the crystal trace should be placed close to the chip side.
- The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.

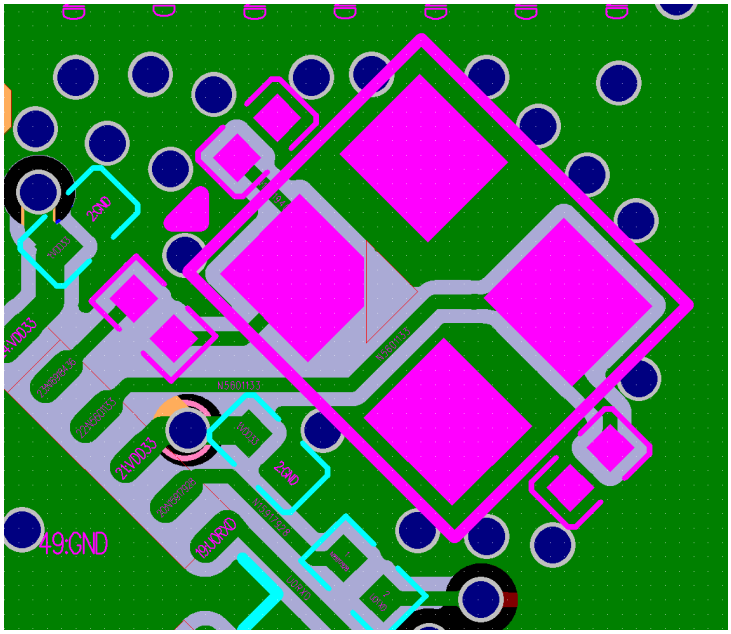

Fig. 7: ESP32-C2 Crystal Layout (without Keep-out Area on Top Layer)

- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

4.5 RF

The RF trace is routed as shown highlighted in pink in Figure *ESP32-C2 RF Layout in a Four-layer PCB Design*.

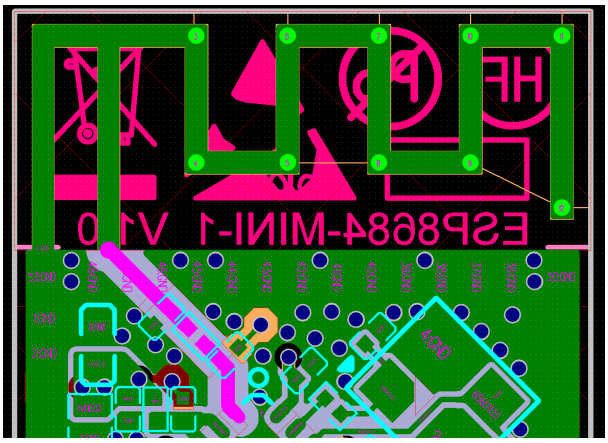

Fig. 8: ESP32-C2 RF Layout in a Four-layer PCB Design

The RF layout should meet the following guidelines:

- A π-type matching circuit should be added to the RF trace and placed close to the chip, in a zigzag.
- The RF trace should have a 50 Ω characteristic impedance. The reference plane is the second layer. For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown below.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Fig. 9: ESP32-C2 PCB Stack-up Design

- Add a stub to the ground at the ground pad of the first matching capacitor to suppress the second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure *ESP32-C2 Stub in a Four-layer PCB Design* is the stub. Note that a stub is not required for package types above 0201.
- The RF trace should have a consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

4.6 UART

Figure *ESP32-C2 UART Layout* shows the UART layout.

The UART layout should meet the following guidelines:

- The series resistor on the U0TXD trace needs to be placed close to the chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.

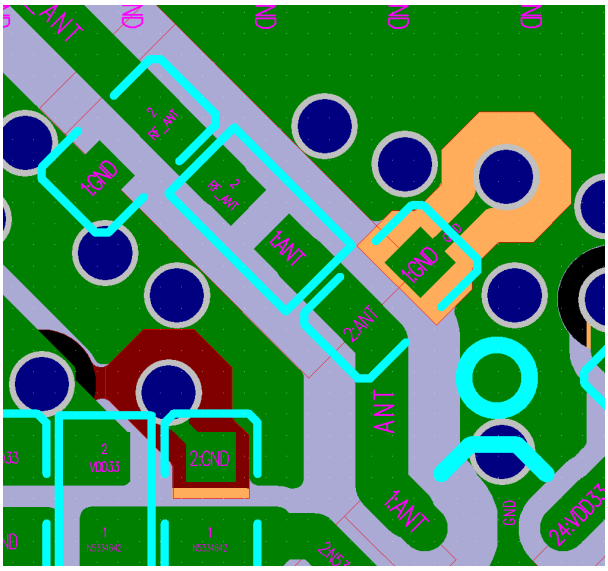

Fig. 10: ESP32-C2 Stub in a Four-layer PCB Design

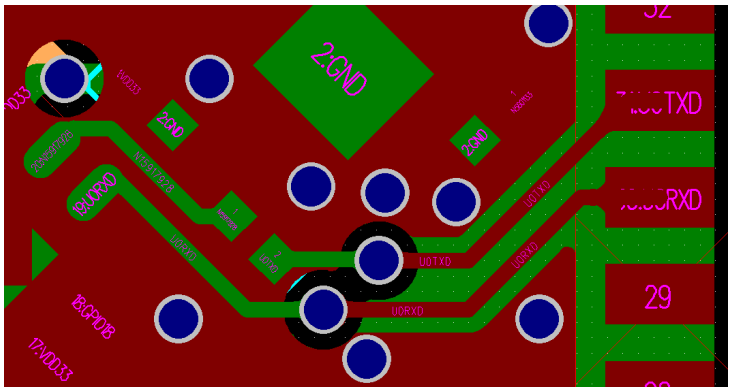

Fig. 11: ESP32-C2 UART Layout

- The UART trace should be surrounded by ground copper and ground vias stitching.

4.7 Typical Layout Problems and Solutions

4.7.1 1. The voltage ripple is not large, but the TX performance of RF is rather poor.

Analysis: The voltage ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-C2 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-C2 sends MCS7@11n packets, and <120 mV when ESP32-C2 sends 11 MHz@11b packets.

Solution: Add a 10 µF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 µF capacitor should be as close to the analog power pin as possible for small and stable voltage ripples.

4.7.2 2. When ESP32-C2 sends data packages, the voltage ripple is small, but RF TX performance is poor.

Analysis: The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution: This problem is caused by improper layout for the crystal and can be solved by re-layout. Please refer to Section *Crystal* for details.

4.7.3 3. When ESP32-C2 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis: The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution: Match the antenna's impedance with the π-type circuit on the RF trace, so that the impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

4.7.4 4. TX performance is not bad, but the RX sensitivity is low.

Analysis: Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution: Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please refer to Section *RF* for details.

Chapter 5

Hardware Development

5.1 ESP32-C2 Modules

For a list of ESP32-C2 modules please check the Modules section on Espressif's official website.

To review module reference designs please check the Documentation section on Espressif's official website.

5.2 ESP32-C2 Development Boards

For a list of the latest designs of ESP32-C2 boards please check the Development Boards section on Espressif's official website.

5.3 Download Guidelines

You can download firmware to ESP32-C2 via UART.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, according to Table *Boot Mode Control*.
2. Power up the chip or module and check the log via the UART0 serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via UART using the Flash Download Tool.
4. After the firmware has been downloaded, pull GPIO9 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.

Note:

- It is advised to download the firmware only after the "waiting for download" log shows via serial ports.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one com port.

Chapter 6

Related Documentation and Resources

- Chip Datasheet (PDF)
- Technical Reference Manual (PDF)
- Chip Errata (PDF)
- Chip Variants
- Modules
- Development Boards
- Espressif KiCad Library
- ESP Product Selector
- Regulatory Certificates
- User Forum (Hardware)
- Technical Support

Chapter 7

Glossary

The glossary contains terms and acronyms that are used in this document.

Term	Description
CLC	Capacitor-Inductor-Capacitor
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Chapter 8

Revision History

8.1 ESP Hardware Design Guidelines v1.0

This is the first version of the ESP Hardware Design Guidelines in HTML format. During the migration from PDF to HTML format, minor updates, improvements, and clarifications were made throughout the documentation.

If you would like to check previous versions of the document, please submit documentation feedback.

Chapter 9

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