

ESP32-S2

Hardware Design Guidelines



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Table of contents

Table of contents	i
1 Latest Version of This Document	3
1.1 About This Document	3
1.1.1 Introduction	3
1.1.2 Latest Version of This Document	3
1.2 Product Overview	3
1.3 Schematic Checklist	4
1.3.1 Overview	4
1.3.2 Power Supply	4
1.3.3 Chip Power-up and Reset Timing	6
1.3.4 Flash and PSRAM	7
1.3.5 Clock Source	7
1.3.6 RF	9
1.3.7 UART	11
1.3.8 SPI	12
1.3.9 Strapping Pins	12
1.3.10 GPIO	13
1.3.11 ADC	15
1.3.12 USB	15
1.3.13 Touch Sensor	16
1.4 PCB Layout Design	16
1.4.1 General Principles of PCB Layout for the Chip	16
1.4.2 Power Supply	16
1.4.3 Crystal	19
1.4.4 RF	20
1.4.5 Flash and PSRAM	22
1.4.6 UART	22
1.4.7 General Principles of PCB Layout for Modules (Positioning a Module on a Base Board)	22
1.4.8 USB	23
1.4.9 Touch Sensor	24
1.4.10 Typical Layout Problems and Solutions	26
1.5 Hardware Development	26
1.5.1 ESP32-S2 Modules	26
1.5.2 ESP32-S2 Development Boards	27
1.5.3 Download Guidelines	27
1.6 Related Documentation and Resources	27
1.7 Glossary	28
1.8 Revision History	28
1.9 Disclaimer and Copyright Notice	29

This document provides guidelines for the [ESP32-S2 SoC](#).

		
Schematic Checklist	PCB Layout Design	Hardware Development

Chapter 1

Latest Version of This Document

Check the link to make sure that you use the latest version of this document: <https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s2/index.html>

1.1 About This Document

1.1.1 Introduction

The hardware design guidelines advise on how to integrate ESP32-S2 into a product. These guidelines will help to achieve optimal performance of your product, ensuring technical accuracy and adherence to Espressif's standards. The guidelines are intended for hardware and application engineers.

The document assumes that you possess a certain level of familiarity with the ESP32-S2 SoC. In case you lack prior knowledge, we recommend utilizing this document in conjunction with the [ESP32-S2 Series Datasheet](#).

1.1.2 Latest Version of This Document

Check the link to make sure that you use the latest version of this document: <https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s2/index.html>

1.2 Product Overview

ESP32-S2 is a system on a chip that integrates the following features:

- Wi-Fi (2.4 GHz band)
- High-performance single core Xtensa® 32-bit LX7 CPU
- Ultra Low Power coprocessor running either RISC-V or FSM core
- Multiple peripherals
- Built-in security hardware
- USB OTG interface

Powered by 40 nm technology, ESP32-S2 provides a robust, highly-integrated platform, which helps meet the continuous demands for efficient power usage, compact design, security, high performance, and reliability. Typical application scenarios for ESP32-S2 include:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Touch and Proximity Sensing

For more information about ESP32-S2, please refer to [ESP32-S2 Series Datasheet](#).

Note: Unless otherwise specified, “ESP32-S2” used in this document refers to the series of chips, instead of a specific chip variant.

1.3 Schematic Checklist

1.3.1 Overview

The integrated circuitry of ESP32-S2 requires only 20 electrical components (resistors, capacitors, and inductors) and a crystal, as well as an SPI flash. The high integration of ESP32-S2 allows for simple peripheral circuit design. This chapter details the schematic design of ESP32-S2.

The following figure shows a reference schematic design of ESP32-S2. It can be used as the basis of your schematic design.

Any basic ESP32-S2 circuit design may be broken down into the following major building blocks:

- *Power supply*
- *Chip power-up and reset timing*
- *Flash and PSRAM*
- *Clock source*
- *RF*
- *UART*
- *Strapping pins*
- *GPIO*
- *ADC*
- *USB*
- *Touch sensor*

The rest of this chapter details the specifics of circuit design for each of these sections.

1.3.2 Power Supply

The general recommendations for power supply design are:

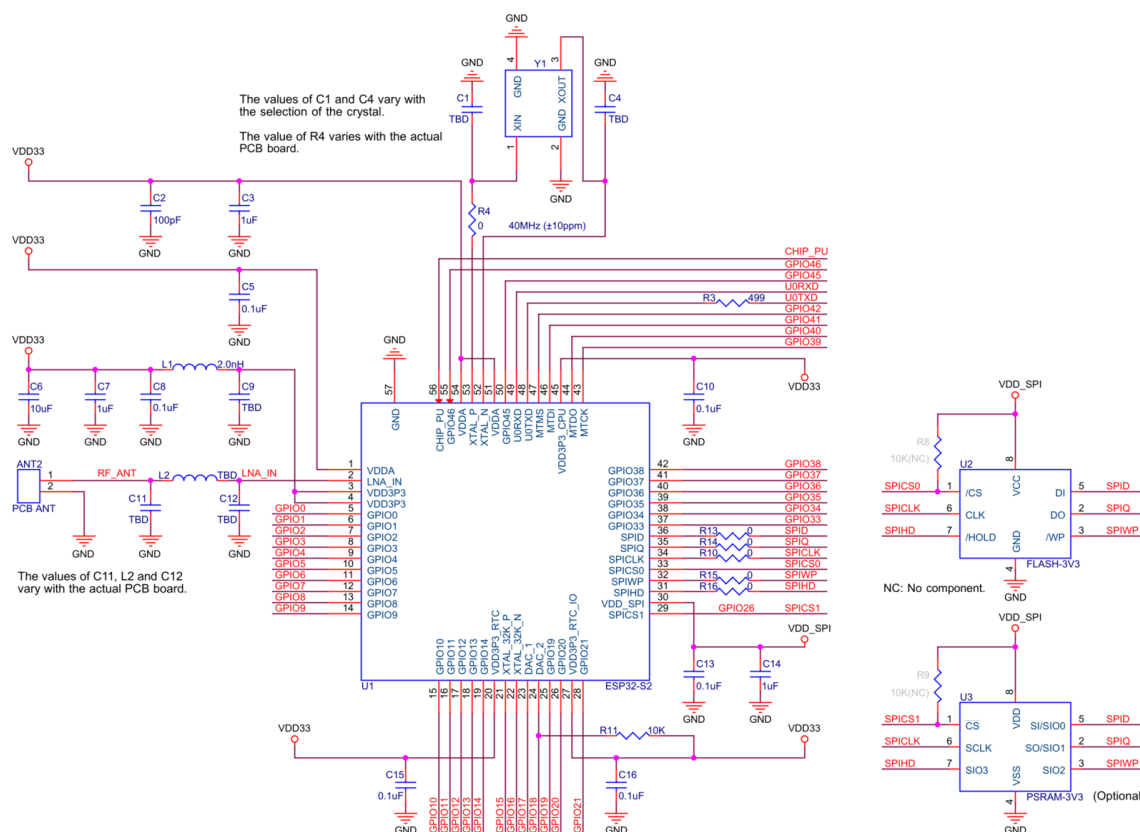


Fig. 1: ESP32-S2 Reference Schematic

- When using a single power supply, the recommended power supply voltage is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add an ESD protection diode at each power entrance.

The power scheme is shown in [ESP32-S2 Series Datasheet](#) > Figure *ESP32-S2 Power Scheme*.

More information about power supply pins can be found in [ESP32-S2 Series Datasheet](#) > Section *Power Supply*.

Digital Power Supply

ESP32-S2 has pin27 VDD3P3_RTC_IO and pin45 VDD3P3_CPU as the digital power supply pin(s) working in a voltage range of 3.0 V ~ 3.6 V and 2.8 V ~ 3.6 V. It is recommended to add an extra 0.1 μ F decoupling capacitor close to the pin(s).

Pin VDD_SPI can serve as the power supply for the external device at either 1.8 V or 3.3 V (default). It is recommended to add extra 0.1 μ F and 1 μ F decoupling capacitors close to VDD_SPI. Please do not add excessively large capacitors.

- When VDD_SPI operates at 1.8 V, it is powered by ESP32-S2's internal LDO. The typical current this LDO can offer is 40 mA.
- When VDD_SPI operates at 3.3 V, it is driven directly by VDD3P3_RTC through a 5 Ω resistor, therefore, there will be some voltage drop from VDD3P3_RTC.

Attention:

- When using VDD_SPI as the power supply pin for in-package or off-package 3.3 V flash/PSRAM, please ensure that VDD3P3_RTC remains above 3.0 V to meet the operating voltage requirements of the flash/PSRAM, considering the voltage drop mentioned earlier.

- Note that VDD3P3_RTC cannot supply power alone; all power supplies must be powered on at the same time.

VDD_SPI can also be driven by an external power supply.

It is recommended to use the VDD_SPI output to supply power to external or internal flash/PSRAM.

Analog Power Supply

ESP32-S2's VDDA, VDD3P3, and VDD3P3_RTC pins are the analog power supply pins, working at 2.8 V ~ 3.6 V.

For VDD3P3, when ESP32-S2 is transmitting signals, there may be a sudden increase in the current draw, causing power rail collapse. Therefore, it is highly recommended to add a 10 μ F capacitor to the power rail, which can work in conjunction with the 0.1 μ F capacitor(s).

Add a LC circuit on the VDD3P3 power rail to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA and above.

1.3.3 Chip Power-up and Reset Timing

ESP32-S2's CHIP_PU pin can enable the chip when it is high and reset the chip when it is low.

When ESP32-S2 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is enabled. Therefore, CHIP_PU needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage V_{IL_nRST} in the range of $(-0.3 \sim 0.25 \times VDD)$ V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible.

Figure *ESP32-S2 Power-up and Reset Timing* shows the power-up and reset timing of ESP32-S2.

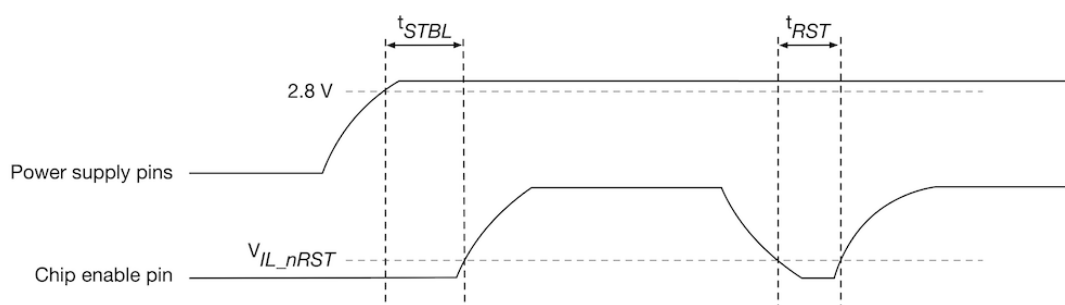


Fig. 2: ESP32-S2 Power-up and Reset Timing

Table *Description of Timing Parameters for Power-up and Reset* provides the specific timing requirements.

Table 1: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Minimum (μ s)
t_{STBL}	Time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	50

Attention:

- CHIP_PU must not be left floating.

- To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually $R = 10\text{ k}\Omega$ and $C = 1\text{ }\mu\text{F}$. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.
- If the user application has one of the following scenarios:
 - Slow power rise or fall, such as during battery charging.
 - Frequent power on/off operations.
 - Unstable power supply, such as in photovoltaic power generation.
 Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:
 - Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
 - Implementing reset functionality through a button or the main controller.

1.3.4 Flash and PSRAM

ESP32-S2 requires in-package or off-package flash to store application firmware and data. In-package PSRAM or off-package PSRAM is optional.

Off-Package Flash and PSRAM

To reduce the risk of software compatibility issues, please use flash and PSRAM models officially validated by Espressif. For detailed model selection, consult the sales or technical support team. If VDD_SPI is used to supply power, make sure to select the appropriate off-package flash and RAM according to the power voltage on VDD_SPI (1.8 V/3.3 V). It is recommended to add zero-ohm resistor footprints in series on the SPI communication lines. These footprints provide flexibility for future adjustments, such as tuning drive strength, mitigating RF interference, correcting signal timing, and reducing noise, if needed.

Currently, the ESP32-S2-WROVER module uses a 4 MB SPI flash and 2 MB PSRAM by default.

The schematic for ESP32-S2 flash and SRAM is shown in Figure [ESP32-S2 Flash and SRAM](#).

1.3.5 Clock Source

ESP32-S2 supports two external clock sources:

- *External crystal clock source (Compulsory)*
- *RTC clock source (Optional)*

External Crystal Clock Source (Compulsory)

The ESP32-S2 firmware only supports 40 MHz crystal.

The circuit for the crystal is shown in Figure [ESP32-S2 Schematic for External Crystal](#). Note that the accuracy of the selected crystal should be within $\pm 10\text{ ppm}$.

Please add a series component on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C4 can be determined according to the formula:

$$C_L = \frac{C1 \times C4}{C1 + C4} + C_{stray}$$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test as below:

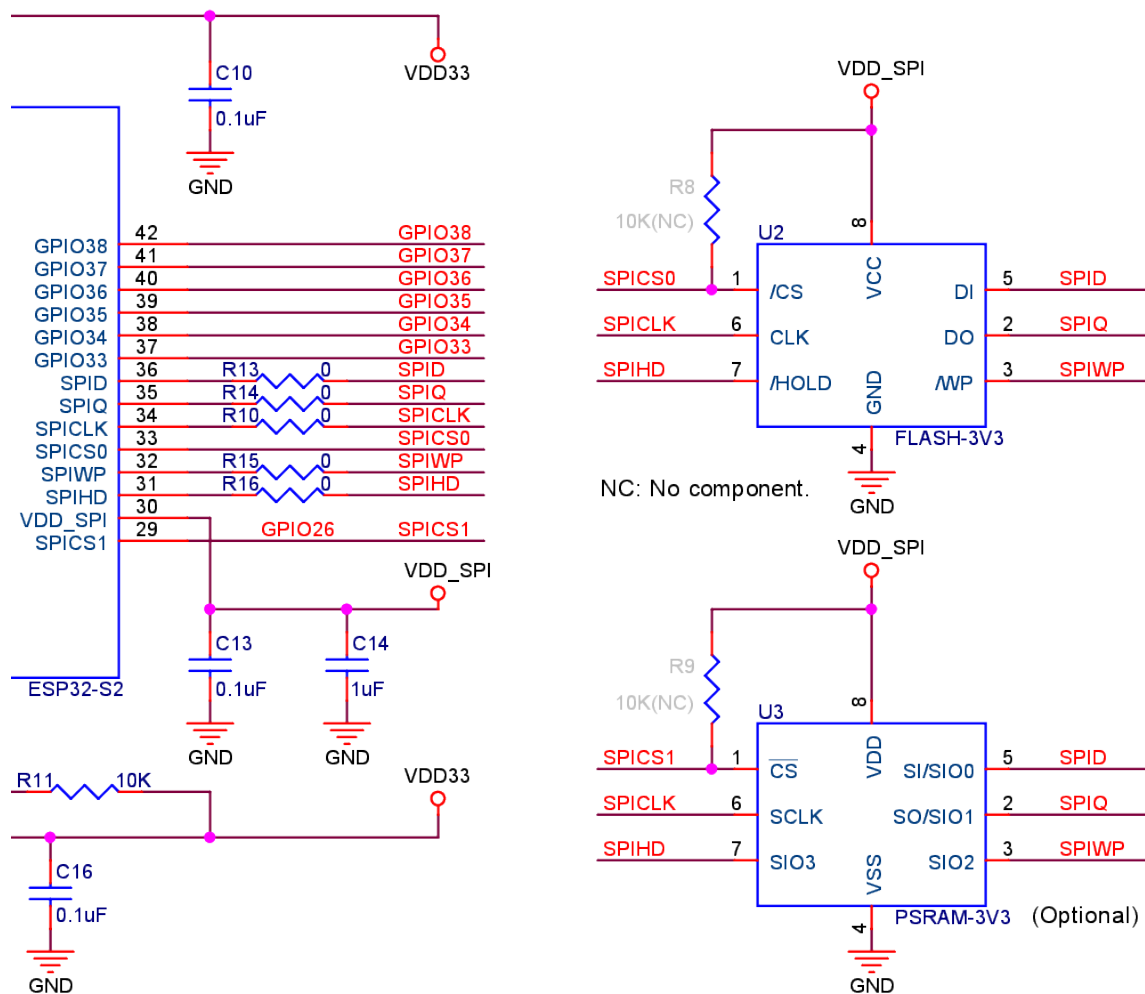


Fig. 3: ESP32-S2 Flash and SRAM

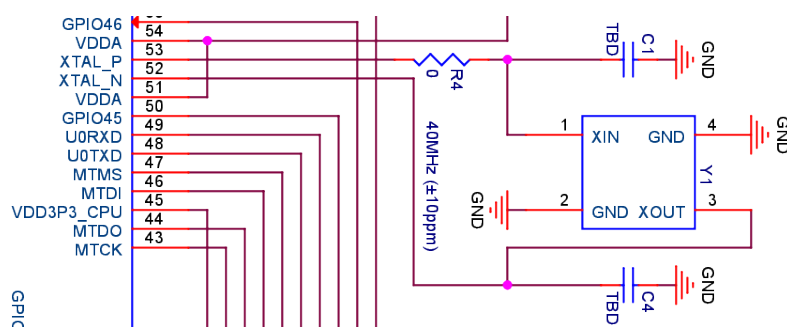


Fig. 4: ESP32-S2 Schematic for External Crystal

1. Select TX tone mode using the [Certification and Test Tool](#).
2. Observe the 2.4 GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ± 10 ppm (recommended) by adjusting the external load capacitance.
 - When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
 - When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
 - External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

If an oscillator is used, its output should be connected to XTAL_P on the chip through a DC blocking capacitor (about 50 pF). XTAL_N can be floating. Please make sure that the oscillator output is stable and its accuracy is within ± 10 ppm. It is also recommended that the circuit design for the oscillator is compatible with the use of the crystal, in case there is a defect in the circuit design, users can still use the crystal. The schematic for the crystal oscillator in ESP32-S2 is shown in Figure [ESP32-S2 Schematic for Crystal Oscillator](#).

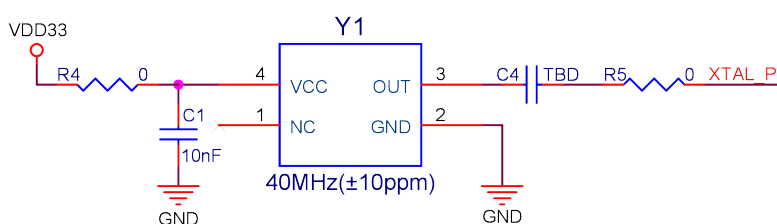


Fig. 5: ESP32-S2 Schematic for Crystal Oscillator

Note:

- Defects in the manufacturing of crystal (for example, large frequency deviation of more than ± 10 ppm, unstable performance within the operating temperature range, etc) may lead to the malfunction of ESP32-S2, resulting in a decrease of the RF performance.
- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

RTC Clock Source (Optional)

ESP32-S2 supports an external 32.768 kHz crystal to act as the RTC clock. The external RTC clock source enhances timing accuracy and consequently decreases average power consumption, without impacting functionality.

Figure [ESP32-S2 Schematic for 32.768 kHz Crystal](#) shows the schematic for the external 32.768 kHz crystal.

Please note the requirements for the 32.768 kHz crystal:

- Equivalent series resistance (ESR) ≤ 70 k Ω .
- Load capacitance at both ends should be configured according to the crystal's specification.

The parallel resistor R is used for biasing the crystal circuit ($5\text{ M}\Omega < R \leq 10\text{ M}\Omega$).

In general, you do not need to populate the resistor.

If the RTC clock source is not required, then the pins for the 32.768 kHz crystal can be used as GPIOs.

1.3.6 RF

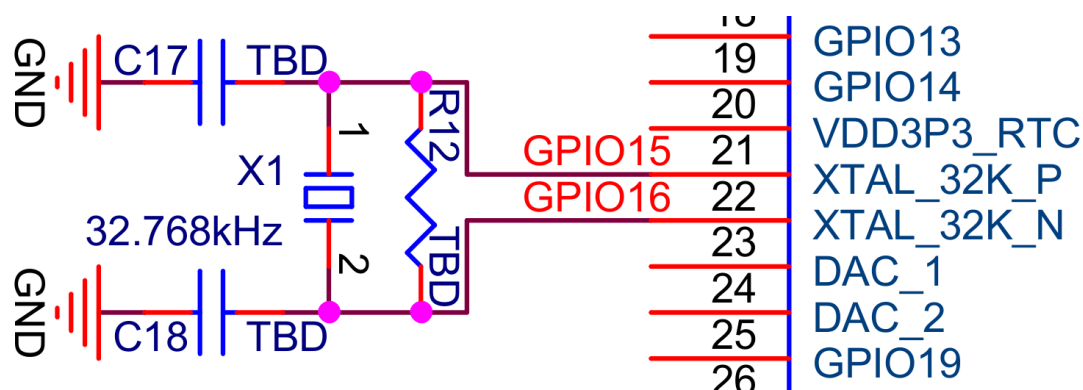


Fig. 6: ESP32-S2 Schematic for 32.768 kHz Crystal

RF Circuit

ESP32-S2's RF circuit is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit. Each part should meet the following requirements:

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. A CLC structure is preferred.
 - The CLC structure is mainly used to adjust the impedance point and suppress harmonics, and a set of LC can be added if space permits.
 - The RF matching circuit is shown in Figure *ESP32-S2 Schematic for RF Matching*.
- For the antenna and the antenna matching circuit, to ensure radiation performance, the antenna's characteristic impedance must be around 50 Ω . Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

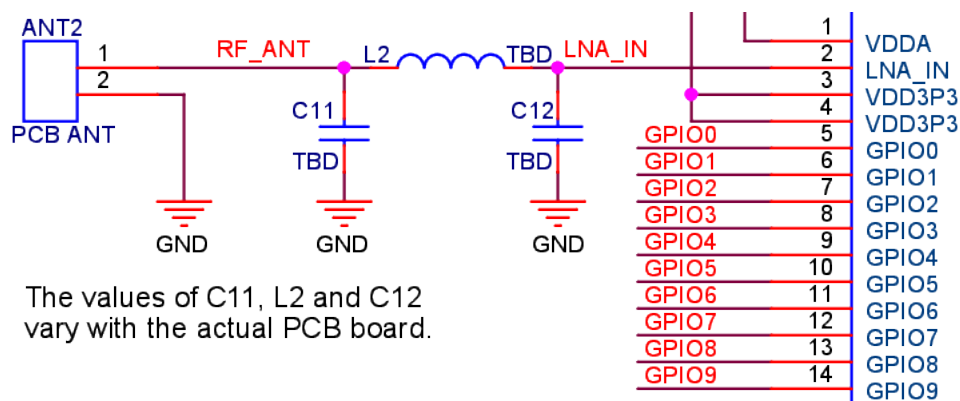


Fig. 7: ESP32-S2 Schematic for RF Matching

RF Tuning

The RF matching parameters vary with the board, so the ones used in Espressif modules could not be applied directly. Follow the instructions below to do RF tuning.

Figure *ESP32-S2 RF Tuning Diagram* shows the general process of RF tuning.

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, the transmission performance is best if the matching impedance is conjugate to the chip impedance. S21 is used to describe the transmission loss of signal from Port 1 to Port 2. If S11 is close to the chip conjugate point 35+j0 and S21 is less than -35 dB at 4.8 GHz and 7.2 GHz, the matching circuit can satisfy transmission requirements.

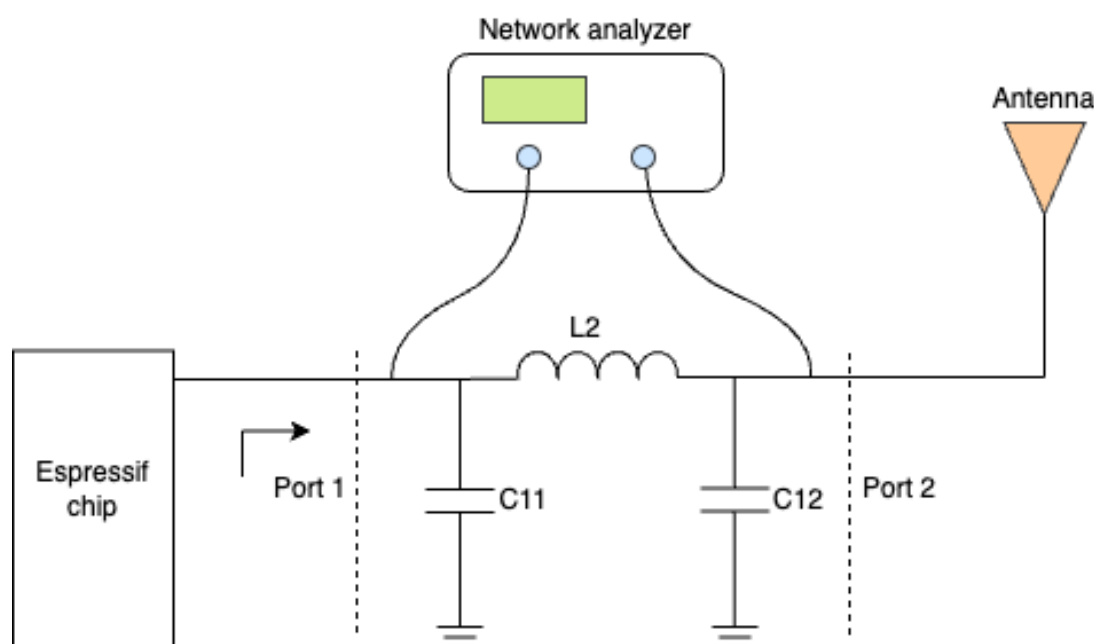


Fig. 8: ESP32-S2 RF Tuning Diagram

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter [PCB Layout Design](#), you can refer to the value ranges in Table [Recommended Value Ranges for Components](#) to debug the matching circuit.

Table 2: Recommended Value Ranges for Components

Reference Designator	Recommended Value Range	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.4 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

If the components are in the 0201 SMD package size, please use a stub in the PCB design of the RF matching circuit near the chip. If the antenna input impedance is not 50 ohm, an additional set of RF matching is recommended for antenna tuning.

Note: If RF function is not required, then the RF pin can be left floating.

1.3.7 UART

Usually, UART0 is used as the serial port for download and log printing. For instructions on download over UART0, please refer to Section [Download Guidelines](#). It is recommended to connect a 499 Ω series resistor to the U0TXD line to suppress harmonics.

If possible, use other UART interfaces as serial ports for communication. For these interfaces, it is suggested to add a series resistor to the TX line to suppress harmonics.

GPIO18 works as U1RXD and is in an uncertain state when the chip is powered on, which may affect the chip's entry into download boot mode. To solve this issue, add an external pull-up resistor.

When using the AT firmware, please note that the UART GPIO is already configured (refer to [Hardware Connection](#)). It is recommended to use the default configuration.

1.3.8 SPI

When using the SPI function, to improve EMC performance, add a series resistor (or ferrite bead) and a capacitor to ground on the SPI_CLK trace. If space allows, it is recommended to also add a series resistor and capacitor to ground on other SPI traces. Ensure that the RC/LC components are placed close to the pins of the chip or module.

1.3.9 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

GPIO0, GPIO45, and GPIO46 are strapping pins.

All the information about strapping pins is covered in [ESP32-S2 Series Datasheet](#) > Chapter *Boot Configurations*.

In this document, we will mainly cover the strapping pins related to boot mode.

After chip reset is released, the combination of GPIO0 and GPIO46 controls the boot mode. See Table [Boot Mode Control](#).

Table 3: Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default Config	1 (Pull-up)	0 (Pull-down)
SPI Boot	1	Any value
Download Boot	0	0
Invalid combination ¹	0	1

Signals applied to the strapping pins should have specific *setup time* and *hold time*. For more information, see Figure [Setup and Hold Times for Strapping Pins](#) and Table [Description of Timing Parameters for Strapping Pins](#).

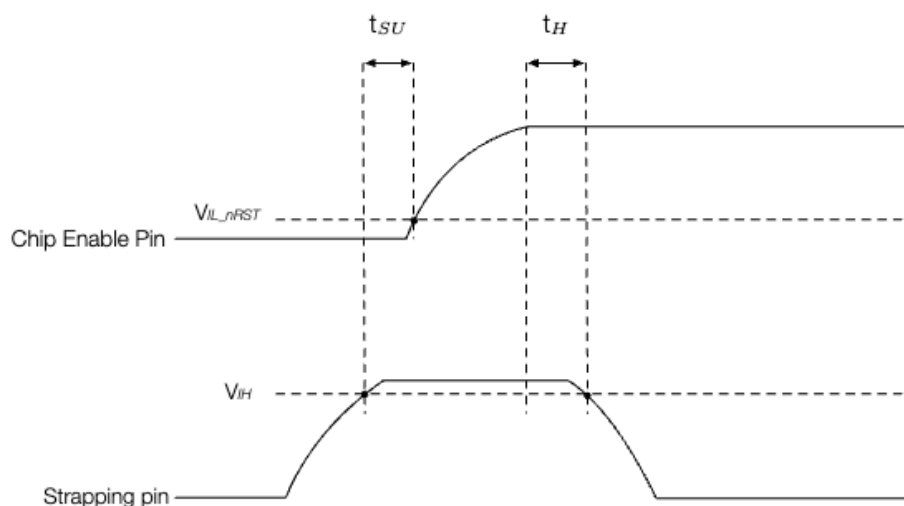


Fig. 9: Setup and Hold Times for Strapping Pins

¹ This combination triggers unexpected behavior and should be avoided.

Table 4: Description of Timing Parameters for Strapping Pins

Parameter	Description	Minimum (ms)
t_{SU}	Time reserved for the power rails to stabilize before the chip enable pin (CHIP_PU) is pulled high to activate the chip.	0
t_H	Time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

Attention:

- It is recommended to place a pull-up resistor at the GPIO0 pin.
- Do not add high-value capacitors at GPIO0, or the chip may enter download mode.

1.3.10 GPIO

The pins of ESP32-S2 can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations (see [ESP32-S2 Series Datasheet](#) > Appendix *ESP32-S2 Consolidated Pin Overview*), whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to [ESP32-S2 Technical Reference Manual](#) > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals have already been routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to [ESP32-S2 Series Datasheet](#) > Section *Peripherals*.

When using GPIOs, please:

- Pay attention to the states of strapping pins during power-up.
- Pay attention to the default configurations of the GPIOs after reset. The default configurations can be found in the table below. It is recommended to add a pull-up or pull-down resistor to pins in the high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.
- Avoid using the pins already occupied by flash/PSRAM.
- GPIO33 ~ GPIO37 work in the same power domain VDD3P3_CPU, which can also be configured to VDD_SPI by software.

Table 5: IO MUX Pin Functions

Pin No	Pin Name	Pin Type	Pin Providing Power	At Reset	After Reset	Digital Function0	RTC	Analog
1	VDDA	Power						
2	LNA_IN	Analog						
3	VDD3P3	Power						
4	VDD3P3	Power						
5	GPIO0	IO	VDD3P3	IEC_IO WPU	IE, WPU	IO MUX	RTC	
6	GPIO1	IO	VDD3P3	IEC_IO	IE	IO MUX	RTC	Analog
7	GPIO2	IO	VDD3P3	IEC_IO	IE	IO MUX	RTC	Analog
8	GPIO3	IO	VDD3P3	IEC_IO		IO MUX	RTC	Analog
9	GPIO4	IO	VDD3P3	IEC_IO		IO MUX	RTC	Analog

continues on next page

Table 5 – continued from previous page

Pin No	Pin Name	Pin Type	Pin Providing Power	At Re-set	After Reset	Digital Function0	RTC	Analog
10	GPIO5	IO	VDD3P3	RTC_IO		IO MUX	RTC	Analog
11	GPIO6	IO	VDD3P3	RTC_IO		IO MUX	RTC	Analog
12	GPIO7	IO	VDD3P3	RTC_IO		IO MUX	RTC	Analog
13	GPIO8	IO	VDD3P3	RTC_IO		IO MUX	RTC	Analog
14	GPIO9	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
15	GPIO10	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
16	GPIO11	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
17	GPIO12	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
18	GPIO13	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
19	GPIO14	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
20	VDD3P3	Power						
21	XTAL_32K	Analog	VDD3P3	RTC_IO		IO MUX	RTC	Analog
22	XTAL_32K	Analog	VDD3P3	RTC_IO		IO MUX	RTC	Analog
23	DAC_1	IO	VDD3P3	RTC_IO	IE	IO MUX	RTC	Analog
24	DAC_2	IO	VDD3P3	RTC_IO	IE, WPU	IO MUX	RTC	Analog
25	GPIO19	IO	VDD3P3	RTC_IO		IO MUX	RTC	Analog
26	GPIO20	IO	VDD3P3	RTC_IO		IO MUX	RTC	Analog
27	VDD3P3	Power						
28	GPIO21	IO	VDD3P3	RTC_IO		IO MUX	RTC	
29	SPICS1	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
30	VDD_SPI	Power						
31	SPIHD	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
32	SPIWP	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
33	SPICS0	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
34	SPI-CLK	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
35	SPIQ	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		
36	SPID	IO	VDD_SPI	IE, WPU	IE, WPU	IO MUX		

continues on next page

Table 5 – continued from previous page

Pin No	Pin Name	Pin Type	Pin Providing Power	At Re-set	After Reset	Digital Function0	RTC	Analog
37	GPIO33	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
38	GPIO34	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
39	GPIO35	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
40	GPIO36	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
41	GPIO37	IO	VDD_SPI / VDD3P3_CPU		IE	IO MUX		
42	GPIO38	IO	VDD3P3_CPU		IE	IO MUX		
43	MTCK	IO	VDD3P3_CPU		IE	IO MUX		
44	MTDO	IO	VDD3P3_CPU		IE	IO MUX		
45	VDD3P3_CPU	Power						
46	MTDI	IO	VDD3P3_CPU		IE	IO MUX		
47	MTMS	IO	VDD3P3_CPU		IE	IO MUX		
48	U0TXD	IO	VDD3P3_CPU	WPU	IE, WPU	IO MUX		
49	U0RXD	IO	VDD3P3_CPU	WPU	IE, WPU	IO MUX		
50	GPIO45	IO	VDD3P3_CPU	WPD	IE, WPD	IO MUX		
51	VDDA	Power						
52	XTAL_N	IO						
53	XTAL_P	IO						
54	VDDA	Power						
55	GPIO46	IO	VDD3P3_CPU	WPD	IE, WPD	IO MUX		
56	CHIP_PU	Analog						
57	GND	Power						

1.3.11 ADC

Please add a 0.1 μ F filter capacitor between ESP pins and ground when using the ADC function to improve accuracy.

1.3.12 USB

ESP32-S2 has a full-speed USB On-The-Go (OTG) peripheral with integrated transceivers. The USB peripheral is compliant with the USB 1.1 specification.

GPIO19 and GPIO20 can be used as D- and D+ of USB respectively. It is recommended to populate 22/33 ohm series resistors between the mentioned pins and the USB connector. Also, reserve a footprint for a capacitor to ground on each trace. Note that both components should be placed close to the chip.

Note that upon power-up, the USB_D+ signal will fluctuate between high and low states. The high-level signal is relatively strong and requires a robust pull-down resistor to drive it low. Therefore, if you need a stable initial state, adding an external pull-up resistor is recommended to ensure a consistent high-level output voltage at startup.

ESP32-S2 also supports leading the GND, RXD, and TXD pins out and connecting them to a USB-to-UART tool for firmware download and log message printing. For details please refer to Section [Download Guidelines](#).

1.3.13 Touch Sensor

When using the touch function, it is recommended to populate a series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 k Ω , preferably 510 Ω . The specific value depends on the actual test results of the product.

The ESP32-S2 touch sensor has a waterproof design and digital filtering function. Note that only GPIO14 (TOUCH14) can drive the shield electrode.

1.4 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-S2 PCB layout using an ESP32-S2 module (see Figure [ESP32-S2 Reference PCB Layout](#)) as an example.

1.4.1 General Principles of PCB Layout for the Chip

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

1.4.2 Power Supply

Four-Layer PCB Design

Figure [ESP32-S2 Power Traces in a Four-Layer PCB Design](#) shows the power traces in a four-layer PCB design.

- A four-layer PCB design is recommended. Whenever possible, route the power traces on the inner layers (not the ground layer) and connect them to the chip pins through vias. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.



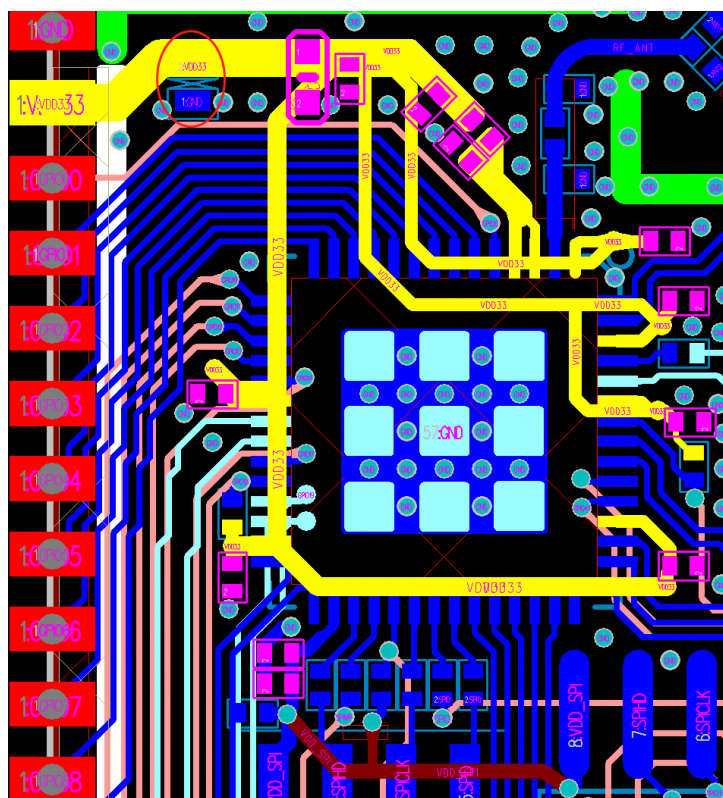


Fig. 11: ESP32-S2 Power Traces in a Four-Layer PCB Design

- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure *ESP32-S2 Power Traces in a Four-Layer PCB Design*. The width of the main power traces should be no less than 25 mil. The width of VDD3P3 at pin3 and pin4 power traces should be no less than 20 mil. The recommended width of other power traces is 10 mil. Ensure the power traces are surrounded by ground copper.
- The red circles in *ESP32-S2 Power Traces in a Four-Layer PCB Design* show ESD protection diodes. Place them close to the power input. Add a 10 μF capacitor before the power trace enters the chip. You can also add a 0.1 μF or 1 μF capacitor in parallel. After that, the power trace can branch out in a star-shaped layout to reduce coupling between different power pins.
- The power supply for pin2 and pin3 is RF related, so please place a 10 μF capacitor for each pin. You can also add a 0.1 μF or 1 μF capacitor in parallel.
- Add a CLC/LC filter circuit near pin2 and pin3 to suppress high-frequency harmonics. The power trace can be routed at a 45-degree angle to maintain distance from adjacent RF traces. Except for the 10 μF capacitor, it is recommended to use 0201 components. This allows the filter circuit for pin2 and pin3 to be placed closer to the pins, with a GND isolation layer separating them from surrounding RF and GPIO traces, while also maximizing the placement of ground vias. Using 0201 components enables placing a via to the bottom layer at the first capacitor near the chip, while maintaining a keep-out area on other layers, further reducing harmonic interference. See Figure *ESP32-S2 Power Traces in a Four-Layer PCB Design*.
- In Figure *ESP32-S2 Power Traces in a Four-Layer PCB Design*, the 10 μF capacitor is shared by the analog power supply VDD3P3 at pin3 and pin4, and the power entrance since the analog power is close to the chip power entrance. If the chip power entrance is not near VDD3P3 at pin3 and pin4, it is recommended to add a 10 μF capacitor to both the chip power entrance and VDD3P3 at pin3 and pin4.
- Place appropriate decoupling capacitors at the rest of the power pins. Ground vias should be added close to the capacitor's ground pad to ensure a short return path.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- The ground pads of the chip and surrounding circuit components should make full contact with the ground copper pour rather than being connected via traces.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to

employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure [ESP32-S2 Power Traces in a Four-Layer PCB Design](#). This helps effectively reduce solder leakage issues when soldering the module EPAD to the substrate.

Two-Layer PCB Design

Figure [ESP32 Power Traces in a Two-Layer PCB Design](#) shows the power traces in a two-layer PCB design.

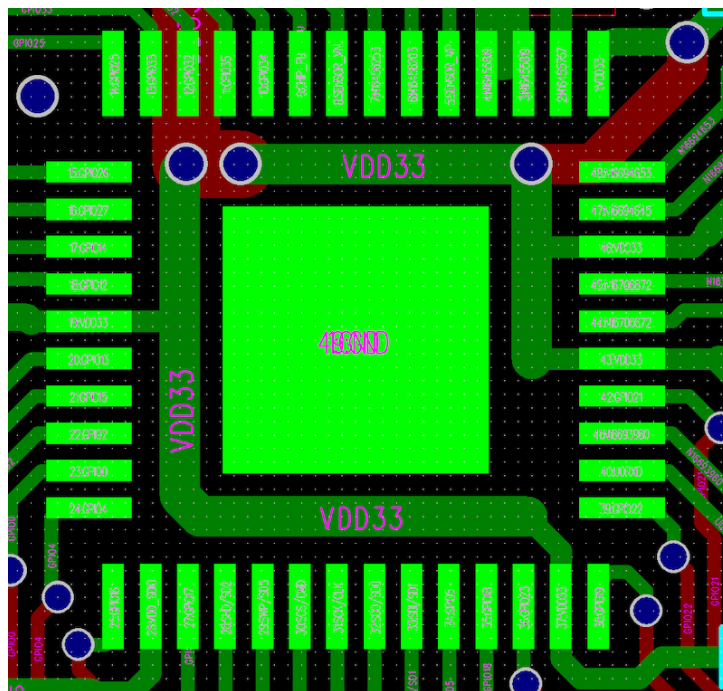


Fig. 12: ESP32 Power Traces in a Two-Layer PCB Design

- For a two-layer design, ensure to provide a continuous reference ground for the chip, RF, and crystal oscillator, as shown in the figure above.
- In the figure above, the trace VDD33 represents the 3.3 V power trace. Unlike a four-layer design, the power trace should be routed on the top layer as much as possible. Therefore, the thermal pad in the center of the chip should be reduced in size, allowing the power trace to pass between the signal pads and the thermal pad. Vias to the bottom layer should only be used when absolutely necessary.
- Other layout considerations are the same as for a four-layer design.
- Note that there are no official two-layer modules. The figure above uses the ESP32 module as an example.

1.4.3 Crystal

Figure [ESP32-S2 Crystal Layout \(without Keep-out Area on Top Layer\)](#) shows the layout for the crystal that is connected to the ground through vias but there is no keep-out area on the top layer for ground isolation.

The layout of the crystal should follow the guidelines below:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 2.0 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces.
- Components in series to the crystal trace should be placed close to the chip side.

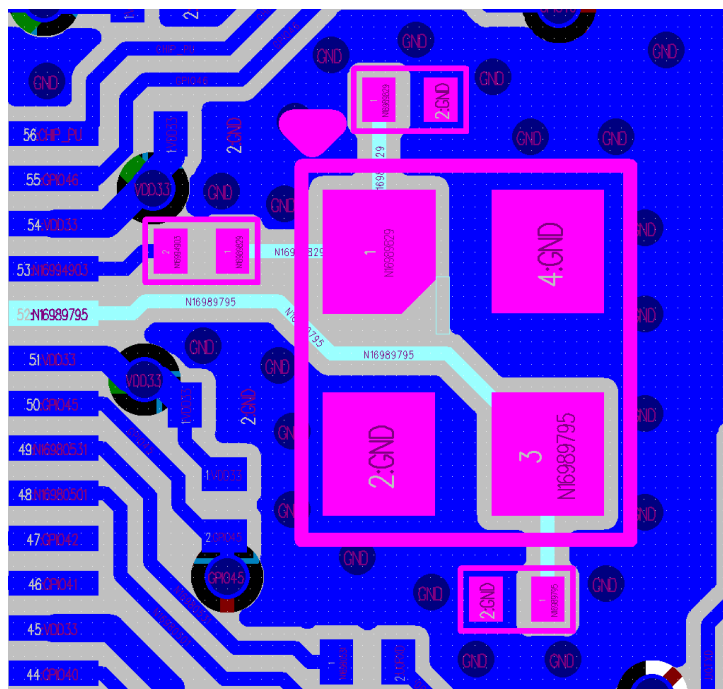


Fig. 13: ESP32-S2 Crystal Layout (without Keep-out Area on Top Layer)

- The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by ground copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

1.4.4 RF

The RF trace is routed as shown highlighted in pink in Figure *ESP32-S2 RF Layout in a Four-layer PCB Design*.

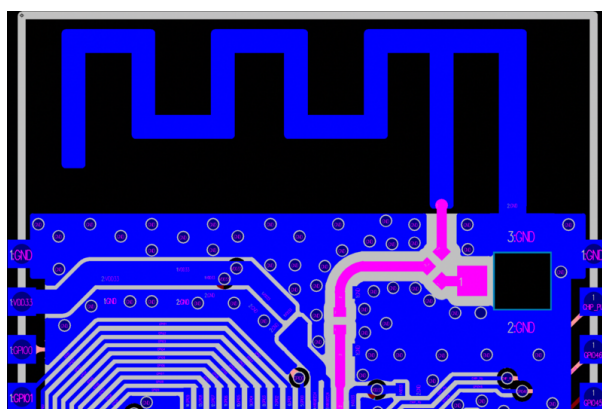


Fig. 14: ESP32-S2 RF Layout in a Four-layer PCB Design

The RF layout should meet the following guidelines:

- The RF trace should have a $50\ \Omega$ characteristic impedance. The reference plane is the layer next to the chip. For designing the RF trace at $50\ \Omega$ impedance, you could refer to the PCB stack-up design shown below.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
CM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	7628 TG150 RC50%		8.22	4.6
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.6
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8.22	4.6
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Fig. 15: ESP32-S2 PCB Stack-up Design

- A CLC matching circuit is required for chip tuning. Please use 0201 components and place them close to the pin in a zigzag. In other words, the two capacitors should not be oriented in the same direction to minimize interference.
- Add a stub on the grounding capacitor near the chip side in the CLC matching circuit to suppress the second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up so that the characteristic impedance of the stub is $100\ \Omega \pm 10\%$. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. Note that a stub is not required for package types of 0402 and above.
- For PCB antennas, make sure to validate them through both simulation and real-world testing on a development board. It is recommended to include an additional CLC matching circuit for antenna tuning. Place this circuit as close to the antenna as possible.
- The RF trace should have a consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

1.4.5 Flash and PSRAM

The layout for flash and PSRAM should follow the guidelines below:

- Place the zero-ohm resistors in series on the SPI lines close to ESP32-S2.
- Route the SPI traces on the inner layer (e.g., the third layer) whenever possible, and add ground copper and ground vias around the clock and data traces of SPI separately.
- If the flash and PSRAM are located far from ESP32-S2, it is recommended to place appropriate decoupling capacitors both at VDD_SPI and near the flash and PSRAM.

Figure *ESP32-S2 Flash and PSRAM Layout* shows an example of flash and PSRAM layout.

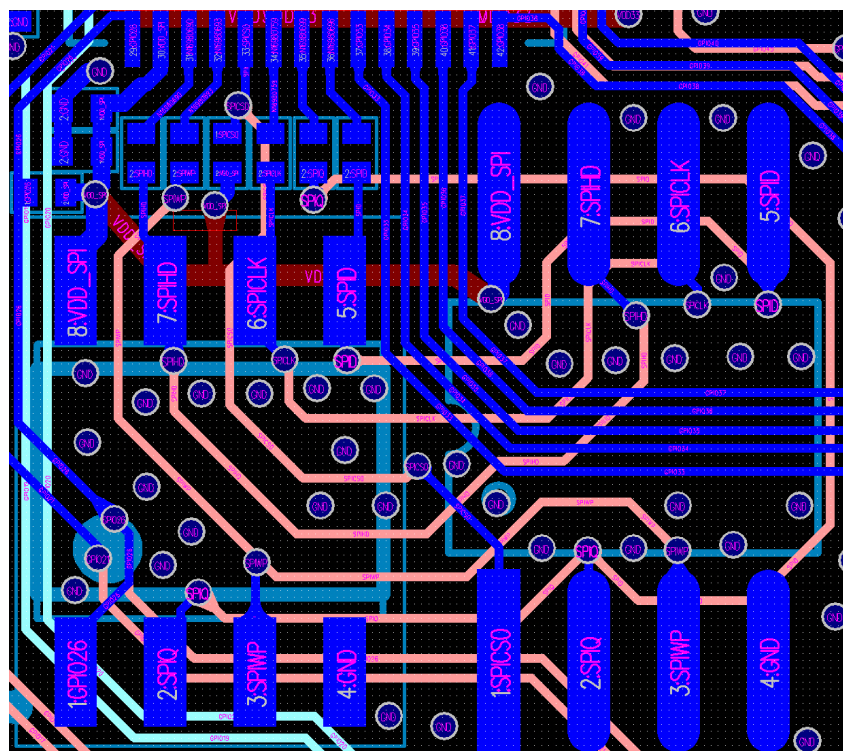


Fig. 16: ESP32-S2 Flash and PSRAM Layout

1.4.6 UART

The UART layout should meet the following guidelines:

- The series resistor on the U0TXD trace needs to be placed close to the chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.
- The UART trace should be surrounded by ground copper and ground vias stitching.

1.4.7 General Principles of PCB Layout for Modules (Positioning a Module on a Base Board)

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the baseboard on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

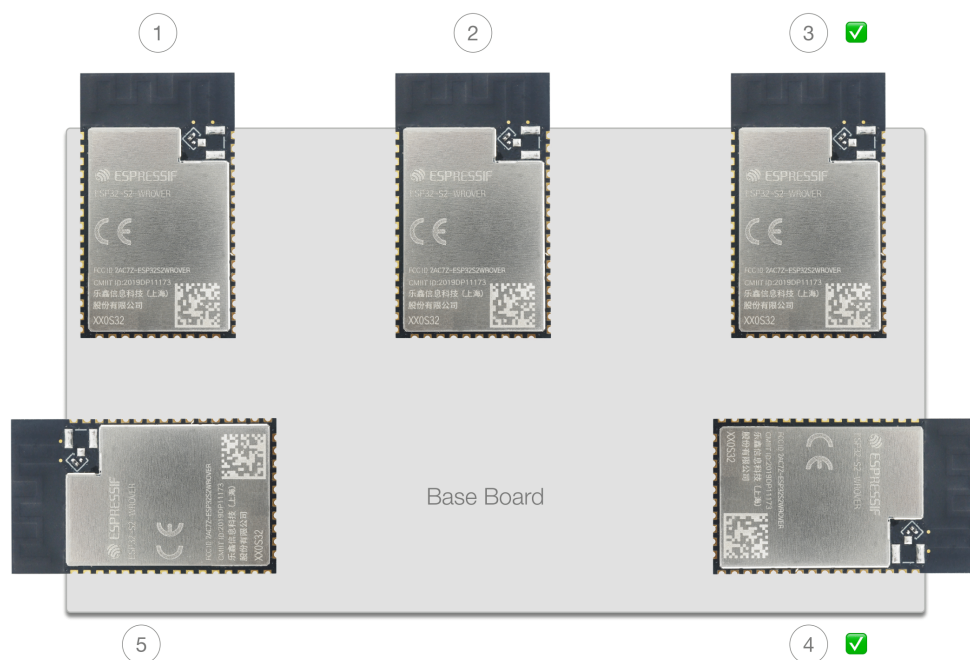


Fig. 17: Placement of ESP32-S2 Modules on Base Board (antenna feed point on the right)

If the PCB antenna cannot be placed outside the board, please ensure a clearance of at least 15 mm (in all directions) around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure *Keepout Zone for ESP32-S2 Module's Antenna on the Base Board* shows the suggested clearance for modules whose antenna feed point is on the right.

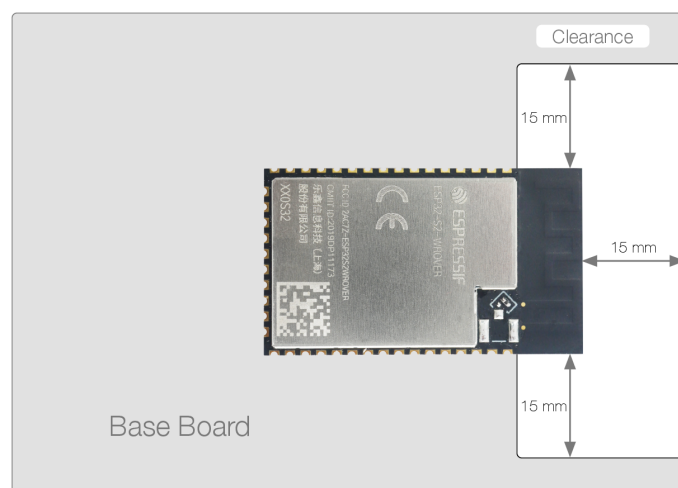


Fig. 18: Keepout Zone for ESP32-S2 Module's Antenna on the Base Board

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification. It is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

1.4.8 USB

The USB layout should meet the following guidelines:

- Reserve space for resistors and capacitors on the USB traces close to the chip side.
- Use differential pairs and route them in parallel at equal lengths. Maintain a differential pair impedance of 90 Ω with a tolerance of $\pm 10\%$.
- USB differential traces should minimize via transitions as much as possible to ensure better impedance control and avoid signal reflections. If vias are necessary, add a pair of ground return vias at each transition point.
- Ensure there is a continuous reference layer (a ground layer is recommended) beneath the USB traces.
- Surround the USB traces with ground copper.

1.4.9 Touch Sensor

ESP32-S2 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip's internal capacitance detection circuit features low noise and high sensitivity. It allows to use touch pads with smaller area to implement the touch detection function. You can also use the touch panel array to detect a larger area or more test points.

Figure *ESP32-S2 Typical Touch Sensor Application* depicts a typical touch sensor application.

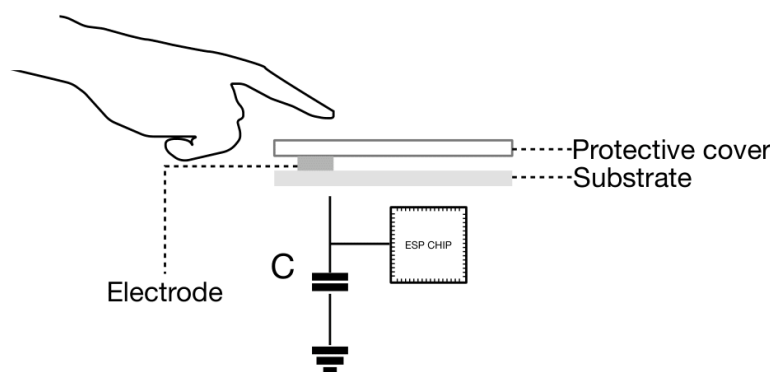


Fig. 19: ESP32-S2 Typical Touch Sensor Application

To prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip are commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

Figure *ESP32-S2 Electrode Pattern Requirements* shows the proper and improper size or shape of electrode. Please note that the examples illustrated in the figure are not of actual scale. It is suggested to use a human fingertip as reference.

PCB Layout

Figure *ESP32-S2 Sensor Track Routing Requirements* illustrates the general guidelines to routing traces. Specifically,

- The trace should be as short as possible and no longer than 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.
- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

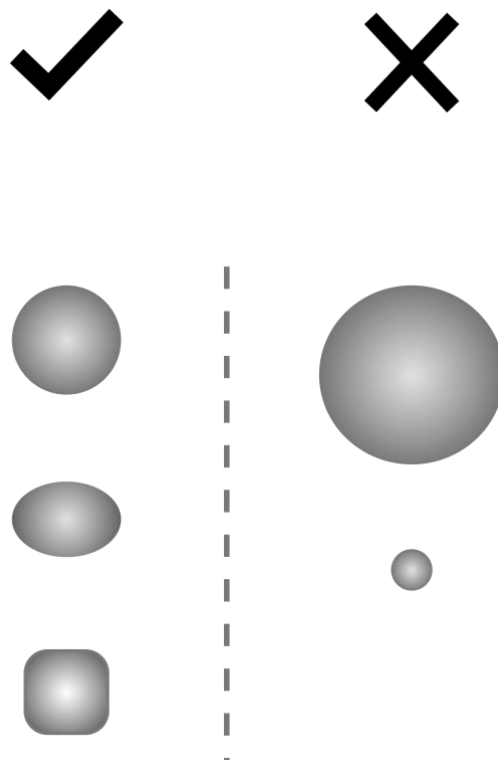


Fig. 20: ESP32-S2 Electrode Pattern Requirements

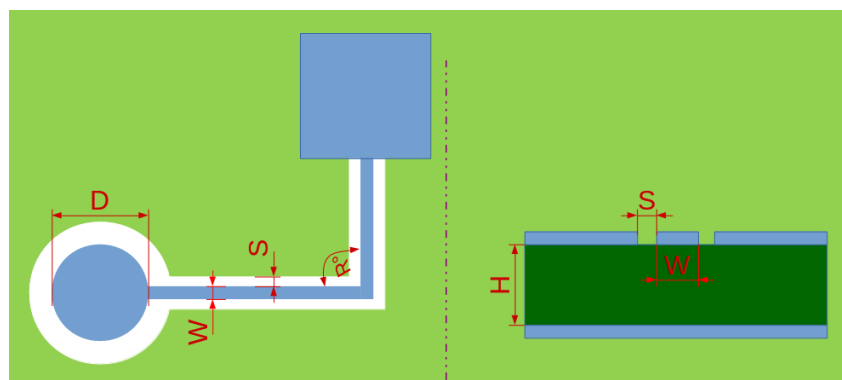


Fig. 21: ESP32-S2 Sensor Track Routing Requirements

Note: For more details on the hardware design of the touch sensor, please refer to [Touch Sensor Application Note](#).

1.4.10 Typical Layout Problems and Solutions

When ESP32-S2 sends data packages, the voltage ripple is small, but RF TX performance is poor.

Analysis: The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution: This problem is caused by improper layout for the crystal and can be solved by re-layout. Please refer to Section [Crystal](#) for details.

When ESP32-S2 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis: The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution: Match the antenna's impedance with the π -type circuit on the RF trace, so that the impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

TX performance is not bad, but the RX sensitivity is low.

Analysis: Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution: Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please refer to Section [RF](#) for details.

1.5 Hardware Development

1.5.1 ESP32-S2 Modules

For a list of ESP32-S2 modules please check the [Modules](#) section on Espressif's official website.

For module reference designs please refer to:

- [Download links](#)

Note: Use the following tools to open the files in module reference designs:

- .DSN files: OrCAD Capture V16.6

- .pcb files: Pads Layout VX.2. If you cannot open the .pcb files, please try importing the .asc files into your software to view the PCB layout.
-

1.5.2 ESP32-S2 Development Boards

For a list of the latest designs of ESP32-S2 boards please check the [Development Boards](#) section on Espressif's official website.

1.5.3 Download Guidelines

You can download firmware to ESP32-S2 via UART.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, according to Table [Boot Mode Control](#).
2. Power up the chip or module and check the log via the UART0 serial port. If the log shows “waiting for download”, the chip or module has entered Joint Download Boot mode.
3. Download your firmware into flash via UART using the [Flash Download Tool](#).
4. After the firmware has been downloaded, pull GPIO0 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.

Note:

- It is advised to download the firmware only after the “waiting for download” log shows via the serial port.
 - Serial tools cannot be used simultaneously with the Flash Download Tool on one COM port.
 - The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip or module to Joint Download Boot mode first by configuring the strapping pin.
 - USB PHY is disabled by the application;
 - USB is secondary developed for other USB functions, e.g., USB host, USB standard device;
 - USB IOs are configured to other peripherals, such as UART and LEDC.
 - It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.
-

1.6 Related Documentation and Resources

- [Chip Datasheet \(PDF\)](#)
- [Technical Reference Manual \(PDF\)](#)
- [Chip Errata \(PDF\)](#)
- [ESP32-S2 Chip Variants](#)
- [Modules](#)
- [ESP32-S2 Development Boards](#)
- [Espressif KiCad Library](#)
- [ESP Product Selector](#)
- [Regulatory Certificates](#)
- [User Forum \(Hardware\)](#)
- [Technical Support](#)

1.7 Glossary

The glossary contains terms and acronyms that are used in this document.

Term	Description
CLC	Capacitor-Inductor-Capacitor
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
Zero-ohm resistor	A zero-ohm resistor acts as a placeholder in the circuit, allowing for the replacement with a higher-ohm resistor based on specific design requirements.

1.8 Revision History

Table 6: Revision History

Date	Version	Release Notes
2025-06-05	v1.6	<ul style="list-style-type: none"> • PCB Layout Design <ul style="list-style-type: none"> – Section USB: Updated descriptions about the USB layout guidelines
2025-05-23	v1.5	<ul style="list-style-type: none"> • PCB Layout Design <ul style="list-style-type: none"> – Section Crystal: Updated descriptions about the crystal layout guidelines
2024-11-15	v1.4	<ul style="list-style-type: none"> • Schematic Checklist <ul style="list-style-type: none"> – Section SPI: Newly added section
2024-10-15	v1.3	<ul style="list-style-type: none"> • Schematic Checklist <ul style="list-style-type: none"> – Section UART: Updated the AT related description
2024-01-09	v1.2	<ul style="list-style-type: none"> • Schematic Checklist <ul style="list-style-type: none"> – Section RF Tuning: Updated RF matching description
2023-12-25	v1.1	<ul style="list-style-type: none"> • PCB Layout Design <ul style="list-style-type: none"> – Section Crystal: Updated crystal PCB layout
2023-12-22	v1.0	Migrated ESP32-S2 Hardware Design Guidelines from PDF to HTML format. During the migration from PDF to HTML format, minor updates, improvements, and clarifications were made throughout the documentation. If you would like to check previous versions of the document, please submit documentation feedback.

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