ESP32-S31

Hardware Design Guidelines

Release master
Espressif Systems
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This document provides guidelines for the ESP32-S31 SoC.

			
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Chapter 1

Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s31/index.html

1.1 About This Document

1.1.1 Introduction

The hardware design guidelines advise on how to integrate ESP32-S31 into a product. These guidelines will help to achieve optimal performance of your product, ensuring technical accuracy and adherence to Espressif's standards. The guidelines are intended for hardware and application engineers.

The document assumes that you possess a certain level of familiarity with the ESP32-S31 SoC. In case you lack prior knowledge, we recommend utilizing this document in conjunction with the ESP32-S31 Series Datasheet.

1.1.2 Latest Version of This Document

Check the link to make sure that you use the latest version of this document: https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s31/index.html

1.2 Product Overview

ESP32-S31 is a system on a chip that integrates the following features:

- 2.4 GHz Wi-Fi 6
- Bluetooth® 5.4 (LE)
- Bluetooth® Classic
- 802.15.4, supporting Thread and Zigbee protocols
- High-performance dual-core 32-bit RISC-V processor
- Multiple peripherals
- Built-in security hardware
- USB 2.0 High-Speed OTG interface
- USB Serial/JTAG controller
- Ethernet MAC interface

Powered by 40 nm technology, ESP32-S31 provides a robust, highly-integrated platform, which helps meet the continuous demands for efficient power usage, compact design, security, high performance, and reliability. Typical application scenarios for ESP32-S31 include:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Wi-Fi + Bluetooth Networking Card
- Touch and Proximity Sensing

For more information about ESP32-S31, please refer to ESP32-S31 Series Datasheet.

Note: Unless otherwise specified, "ESP32-S31" used in this document refers to the series of chips, instead of a specific chip variant.

1.3 Schematic Checklist

1.3.1 Overview

The integrated circuitry of ESP32-S31 requires only 30 electrical components (resistors, capacitors, and inductors) and a crystal, as well as an SPI flash. The high integration of ESP32-S31 allows for simple peripheral circuit design. This chapter details the schematic design of ESP32-S31.

The following figure shows a reference schematic design of ESP32-S31. It can be used as the basis of your schematic design.

Note: The core circuit is the minimum required circuit. Please do not remove components arbitrarily.

Any basic ESP32-S31 circuit design may be broken down into the following major building blocks:

- *Power supply*
- *Chip power-up and reset timing*
- *Flash and PSRAM*
- *Clock source*
- *RF*
- *UART*
- *SPI*
- *Strapping pins*
- *External capacitor*

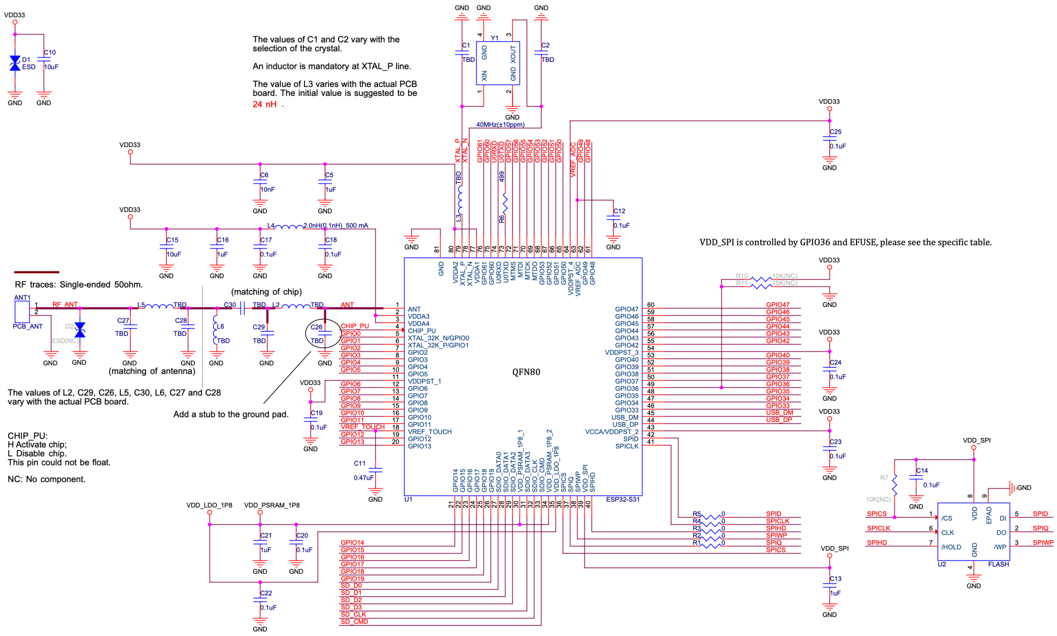

Fig. 1: ESP32-S31 Reference Schematic

- *GPIO*
- *ADC*
- *SD/MMC Host Controller*
- *USB*
- *Touch sensor*
- *Ethernet MAC*
- *LCD and Camera Controller*

The rest of this chapter details the specifics of circuit design for each of these sections.

1.3.2 Power Supply

The general recommendations for power supply design are:

- When using a single power supply, the recommended power supply voltage is 3.3 V and the output current is no less than 800 mA.
- It is suggested to add an ESD protection diode and at least 10 µF capacitor at the main power entrance (where the external power supply enters the PCB).

The power scheme is shown in Figure *ESP32-S31 Power Scheme*.

More information about power supply pins can be found in ESP32-S31 Series Datasheet > Section *Power Supply*.

Digital Power Supply

- Pin VDDPST_1 of ESP32-S31 is a power supply input pin associated with the digital LP power domain, with an operating voltage range of 3.0 V ~ 3.6 V. It is recommended to add a 0.1 µF capacitor close to this power supply pin in the circuit.
- Pins VDDPST_3 and VDDPST_4 are power supply input pins associated with the digital HP power domain, with an operating voltage range of 3.0 V ~ 3.6 V. It is recommended to add a 0.1 µF capacitor close to each of these power supply pins in the circuit.

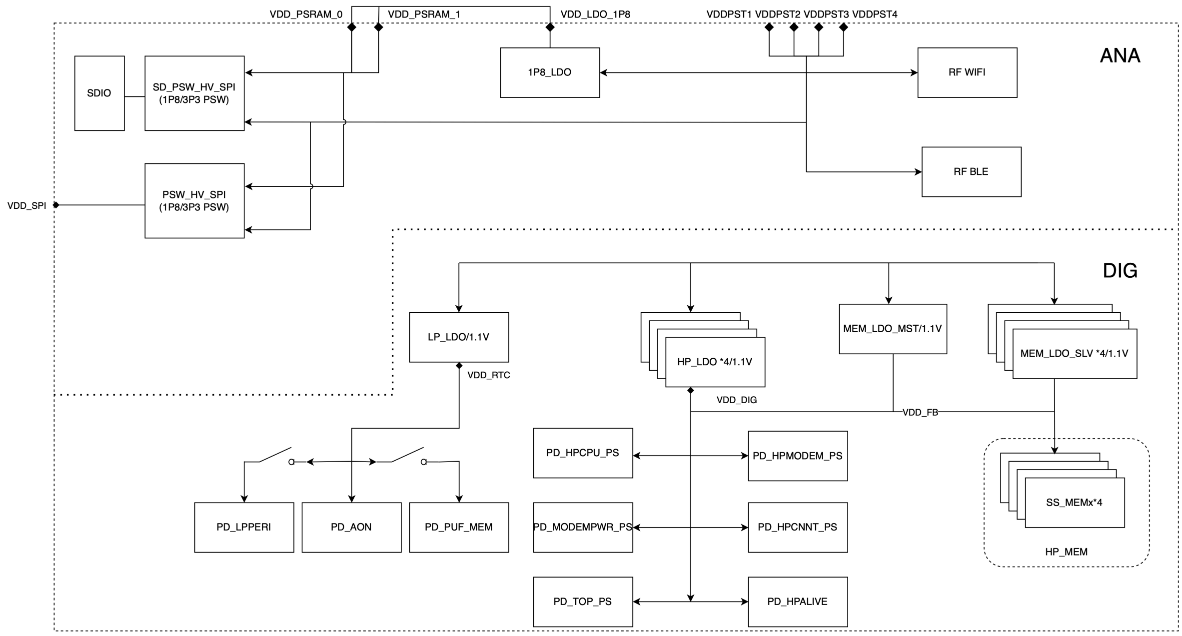

Fig. 2: ESP32-S31 Power Scheme

- Pin VCCA/VDDPST_2 is a power supply input pin associated with USB_PHY and the digital HP power domain, with an operating voltage range of 3.0 V ~ 3.6 V. It is recommended to add a 0.1 µF capacitor close to this power supply pin in the circuit.
- Pin VDD_SPI is a power supply input/output pin associated with the flash power domain. It is recommended to use the VDD_SPI output power to supply the off-package flash. It is recommended to add 0.1 µF and 1 µF decoupling capacitors close to this power supply pin and the flash.

Currently, pin VDD_SPI can only output 3.3 V. Please add an external pull-up resistor on GPIO36.

- Pins VDD_PSRAM_1P8_1 and VDD_PSRAM_1P8_2 are power supply input pins associated with the PSRAM power domain. It is recommended to add 0.1 µF and 1 µF capacitors close to each of these power supply pins in the circuit.
- Pin VDD_LDO_1P8 is a power output pin that can be used to supply in-package PSRAM, off-package flash, and internal SD GPIO.

It is recommended to use the VDD_LDO_1P8 output power to supply the in-package PSRAM, that is, connect VDD_PSRAM_1P8_1 and VDD_PSRAM_1P8_2 to VDD_LDO_1P8.

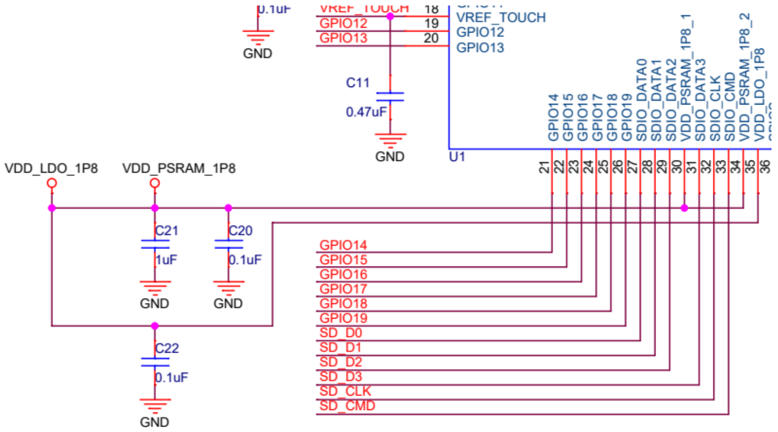

Fig. 3: ESP32-S31 Series Chip PSRAM Power Schematic

Analog Power Supply

ESP32-S31's VDDA1 to VDDA4 pins are the analog power supply pins, working at 3.0 V ~ 3.6 V.

It is recommended to add 10 nF and 1 µF capacitors close to the VDDA1 and VDDA2 power supply pins in the circuit.

For VDDA3 and VDDA4, when ESP32-S31 is transmitting signals, there may be a sudden increase in the current draw, causing power rail collapse. Therefore, it is highly recommended to add a 10 µF capacitor to the power rail, which can work in conjunction with the 1 µF capacitor(s) or other capacitors.

It is suggested to add an extra 10 µF capacitor at the main power entrance. If the main power entrance is close to VDDA3 and VDDA4, then the two 10 µF capacitors can be merged into one.

Add an LC circuit to the VDDA3 and VDDA4 power rail to suppress high-frequency harmonics. The inductor's rated current is preferably 500 mA and above.

For the remaining capacitor circuits, please refer to *ESP32-S31 Reference Schematic*.

1.3.3 Chip Power-up and Reset Timing

ESP32-S31's CHIP_PU pin can enable the chip when it is high and reset the chip when it is low.

When ESP32-S31 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is enabled. Therefore, CHIP_PU needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage V_{IL_nRST} in the range of (–0.3 ~ 0.15 × VDDPST_1) V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible.

Figure *ESP32-S31 Power-up and Reset Timing* shows the power-up and reset timing of ESP32-S31.

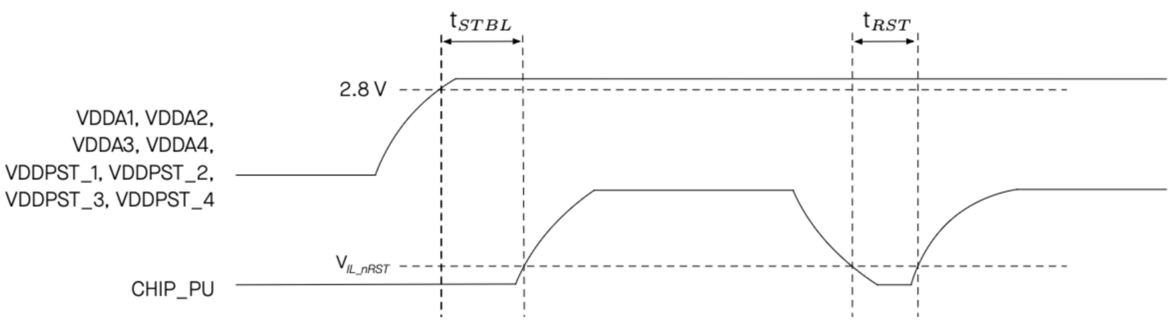

Fig. 4: ESP32-S31 Power-up and Reset Timing

Table *Description of Timing Parameters for Power-up and Reset* provides the specific timing requirements.

Table 1: Description of Timing Parameters for Power-up and Reset

Parameter	Description	Minimum (ms)
t_{STBL}	Time required for VDDA1, VDDA2, VDDA3, VDDA4, VDDPST_1, VDDPST_2, VDDPST_3, and VDDPST_4 to stabilize before the CHIP_PU pin is pulled high to activate the chip	1
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	1

Attention:

- CHIP_PU must not be left floating.
- To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.
- If the user application has one of the following scenarios:
  - Slow power rise or fall, such as during battery charging.
  - Frequent power on/off operations.
  - Unstable power supply, such as in photovoltaic power generation.

  Then, the RC circuit alone may not meet the timing requirements, which may prevent the chip from entering normal operating mode or cause flash erase operations to occasionally fail to complete. In this case, please reserve a power monitor chip to reset the chip when the power supply is abnormal, and the threshold of the power monitor chip is recommended to be around 3.0 V.

1.3.4 Flash and PSRAM

Currently, ESP32-S31 firmware only supports NOR flash.

ESP32-S31 requires off-package flash to store application firmware and data. ESP32-S31 supports connecting flash via SPI, Dual SPI, Quad SPI/QPI, and other interface modes, with a maximum supported flash size of 256 MB.

ESP32-S31 has in-package octal 1.8 V PSRAM, but the PSRAM pins are not bonded out.

Table *Pin Mapping Between Chip and Off-Package Flash* lists the pin-to-pin mapping between the chip and off-package flash in all SPI modes.

Table 2: Pin Mapping Between Chip and Off-Package Flash

Pin No.	Pin Name	Single SPI	Dual SPI	Quad SPI/QPI
36	SPICS	CS#	CS#	CS#
37	SPIQ	DO	DO	DO
38	SPIWP	WP#	WP#	WP#
40	SPIHD	HOLD#	HOLD#	HOLD#
41	SPICLK	CLK	CLK	CLK
42	SPID	DI	DI	DI

To reduce the risk of software compatibility issues, it is recommended to use flash models officially validated by Espressif. For detailed model selection, consult the sales or technical support team. It is recommended to add zero-ohm resistor footprints in series on the SPI communication lines as shown in Figure *ESP32-S31 Schematic for External Flash*. These footprints provide flexibility for future adjustments, such as tuning drive strength, mitigating RF interference, correcting signal timing, and reducing noise, if needed.

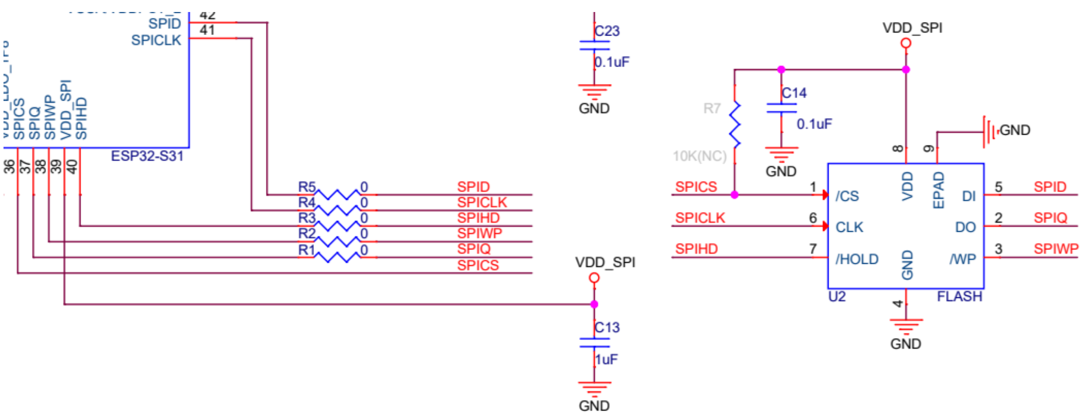

Fig. 5: ESP32-S31 Schematic for External Flash

1.3.5 Clock Source

ESP32-S31 supports two external clock sources:

- *External crystal clock source (Compulsory)*
- *RTC clock source (Optional)*

External Crystal Clock Source (Compulsory)

The ESP32-S31 firmware only supports 40 MHz crystal.

The circuit for the crystal is shown in Figure *ESP32-S31 Schematic for External Crystal*. Note that the accuracy of the selected crystal should be within ±10 ppm.

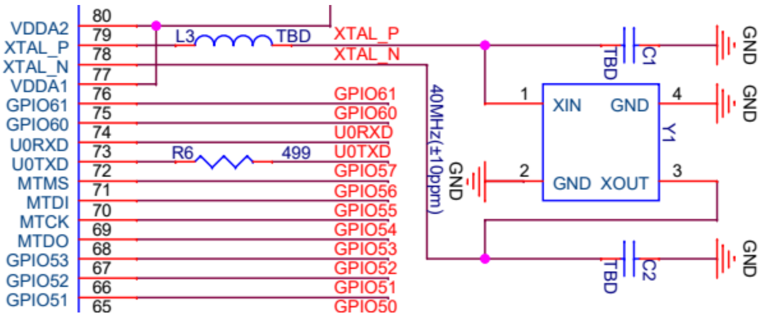

Fig. 6: ESP32-S31 Schematic for External Crystal

A series inductor must be added on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH (0201). This inductor is required for normal system startup. Even if RF function is not used, this inductor is still required. It can also be used to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be confirmed after testing.

The initial values of external capacitors C1 and C2 can be determined according to the formula:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C2 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.
2. Observe the 2.4 GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.

- When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
- When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
- External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

Note:

- Defects in the manufacturing of crystal (for example, large frequency deviation of more than ±10 ppm, unstable performance within the operating temperature range, etc) may lead to the malfunction of ESP32-S31, resulting in a decrease of the RF performance.
- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

RTC Clock Source (Optional)

ESP32-S31 supports an external 32.768 kHz crystal to act as the RTC clock. The external RTC clock source enhances timing accuracy and consequently decreases average power consumption, without impacting functionality.

Figure *ESP32-S31 Schematic for 32.768 kHz Crystal* shows the schematic for the external 32.768 kHz crystal.

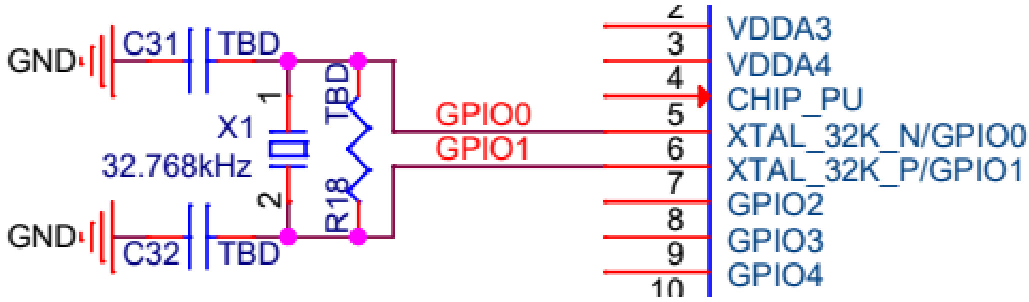

Fig. 7: ESP32-S31 Schematic for 32.768 kHz Crystal

Please note the requirements for the 32.768 kHz crystal:

- Equivalent series resistance (ESR) ≤ 70 kΩ.
- Load capacitance at both ends should be configured according to the crystal's specification.

The parallel resistor R is used for biasing the crystal circuit (5 MΩ < R ≤ 10 MΩ).

In general, you do not need to populate the resistor.

If the RTC clock source is not required, then the pins for the 32.768 kHz crystal can be used as GPIOs.

1.3.6 RF

RF Circuit

ESP32-S31's RF circuit is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit. Each part should meet the following requirements:

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. A CLCCL structure is preferred.
  - The CLCCL structure forms a bandpass filter, which is mainly used to adjust impedance points, suppress high-frequency harmonics and low-frequency noise, and improve anti-interference capability.
  - The RF matching circuit is shown in Figure *ESP32-S31 Schematic for RF Matching*.
- For the antenna and the antenna matching circuit, to ensure radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna.
- It is recommended that the overall matching circuit include at least two CLC structures.

RF Tuning

The RF matching parameters vary with the board, so the ones used in Espressif modules could not be applied directly. Follow the instructions below to do RF tuning.

Figure *ESP32-S31 RF Tuning Diagram* shows the general process of RF tuning.

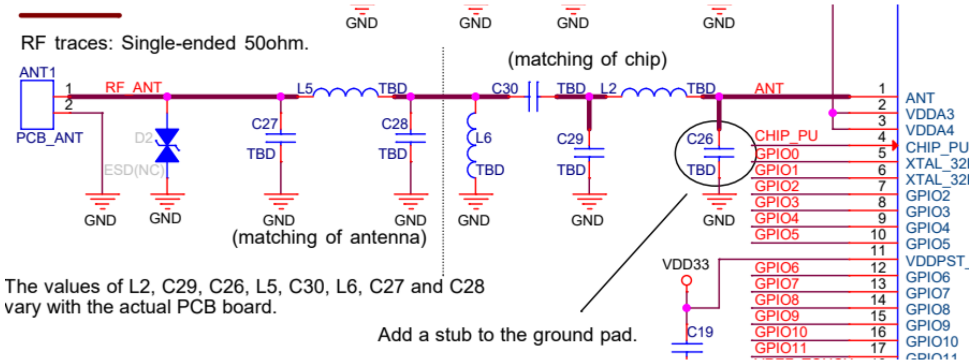

Fig. 8: ESP32-S31 Schematic for RF Matching

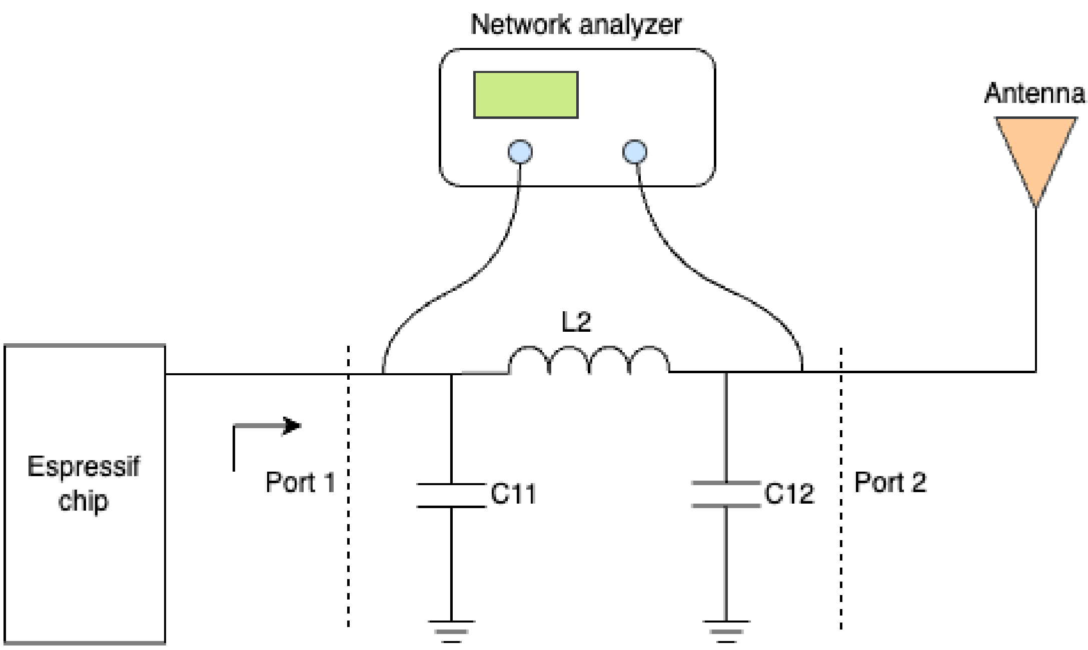

Fig. 9: ESP32-S31 RF Tuning Diagram

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, the transmission performance is best if the matching impedance is conjugate to the chip impedance. S21 is used to describe the transmission loss of signal from Port 1 to Port 2. If S11 is close to the chip conjugate point 40+j0 and S21 is less than -35 dB at 4.8 GHz and 7.2 GHz, the matching circuit can satisfy transmission requirements.

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter *PCB Layout Design*, you can refer to the value ranges in Table *Recommended Value Ranges for Components* to debug the matching circuit.

Table 3: Recommended Value Ranges for Components

Reference Designator	Recommended Value Range	Serial No.
C11	1.2 ~ 1.8 pF	GRM0335C1H1RXBA01D
L2	2.0 ~ 3.0 nH	LQP03TN2NXB02D
C12	1.8 ~ 1.2 pF	GRM0335C1H1RXBA01D

Please use 0201 packages for RF matching components and add a stub to the first capacitor in the matching circuit at the chip end.

Note: If RF function is not required, it is recommended not to initialize the RF stack in firmware. In this case, the RF pin can be left floating. However, if RF function is enabled, make sure an antenna is connected. Operation without an antenna may result in unstable behavior or potential damage to the RF circuit.

1.3.7 UART

ESP32-S31 includes 4 UART interfaces, UART0 ~ UART3. U0TXD and U0RXD are GPIO58 and GPIO59 by default. Other UART signals can be mapped to any available GPIOs via the GPIO matrix.

ESP32-S31 also has one LP UART, which can be configured to any LP GPIO pin.

Usually, UART0 is used as the serial port for download and log printing. For instructions on download over UART0, please refer to Section *Download Guidelines*. It is recommended to connect a 499 Ω series resistor to the U0TXD line to suppress harmonics.

For application communication, use UART interfaces other than UART0 if possible. Add a series resistor on the TX line to suppress harmonics.

1.3.8 SPI

When using the SPI function, to improve EMC performance, add a series resistor (or ferrite bead) and a capacitor to ground on the SPI_CLK trace. If space allows, it is recommended to also add a series resistor and capacitor to ground on other SPI traces. Ensure that the RC/LC components are placed close to the pins of the chip or module.

1.3.9 Strapping Pins

At each startup or reset, a chip requires some initial configuration parameters, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins work as normal function pins.

GPIO37, GPIO60, and GPIO61 are strapping pins.

All the information about strapping pins is covered in ESP32-S31 Series Datasheet > Chapter *Boot Configurations*.

In this section, we will mainly cover the strapping pins related to boot mode.

After chip reset is released, the combination of GPIO60 and GPIO61 controls the boot mode. See Table *Chip Boot Mode Control*.

Table 4: Chip Boot Mode Control

Boot Mode	GPIO61	GPIO60
SPI Boot (default)	**1**	Any value
Joint Download Boot	0	1

Note:

- **Bold** indicates default values and default configurations.
- The Joint Download Boot mode supports the following download methods:
  - USB-Serial-JTAG Download Boot
  - USB-OTG Download Boot
  - UART Download Boot
  - GPSPI Download Boot

In addition to SPI Boot and Joint Download Boot modes, ESP32-S31 also supports SPI Download Boot mode.

Signals applied to the strapping pins should have specific *setup time* and *hold time*. For more information, see Figure *Setup and Hold Times for Strapping Pins* and Table *Description of Timing Parameters for Strapping Pins*.

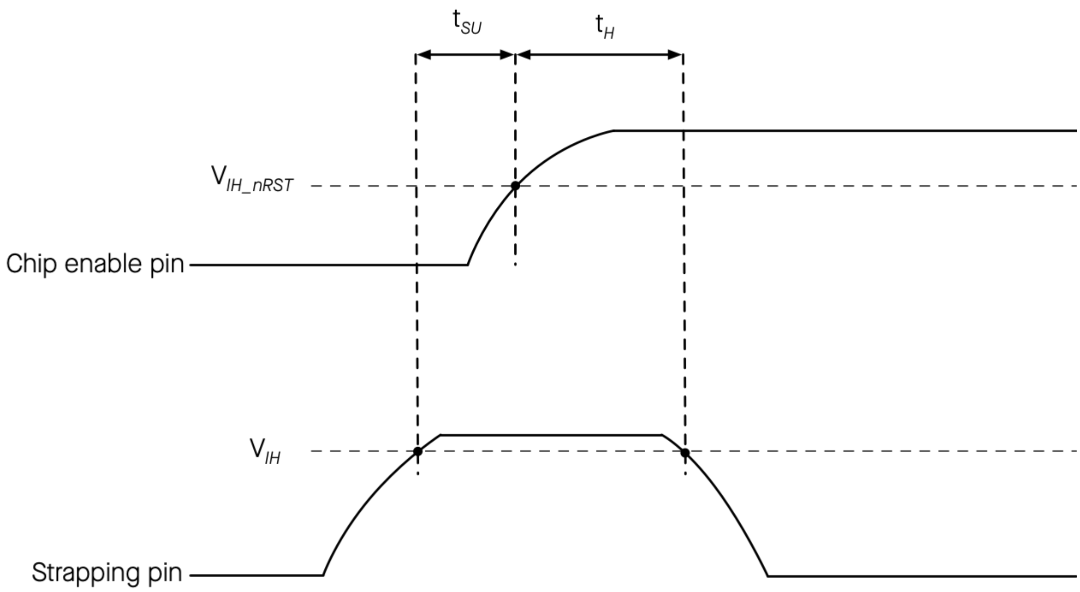

Fig. 10: Setup and Hold Times for Strapping Pins

Table 5: Description of Timing Parameters for Strapping Pins

Parameter	Description	Minimum (ms)
t_{SU}	Time reserved for the power rails to stabilize before the chip enable pin (CHIP_PU) is pulled high to activate the chip.	0
t_H	Time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

> **Attention:**
>
> - It is recommended to place a pull-up resistor at the GPIO61 pin.
> - Do not add high-value capacitors at GPIO61, or the chip may enter download mode.

1.3.10 External Capacitor

ESP32-S31 has the following pins that require external capacitors:

- VREF_TOUCH is the TOUCH reference voltage capacitor pin. It is recommended to add a 0.47 µF capacitor close to this pin in the circuit. If the TOUCH function is not used, this pin can be left floating.
- VREF_ADC is the ADC reference voltage capacitor pin. It is recommended to add a 0.1 µF capacitor close to this pin in the circuit. If the ADC function is not used, this pin can be left floating.

1.3.11 GPIO

The pins of ESP32-S31 can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations (see ESP32-S31 Series Datasheet > Appendix *ESP32-S31 Consolidated Pin Overview*), whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to ESP32-S31 Technical Reference Manual > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals have already been routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to ESP32-S31 Series Datasheet > Section *Peripherals*.

When using GPIOs, please:

- Pay attention to the states of strapping pins during power-up.
- Pay attention to the default GPIO configurations after reset (see the table below). For unused pins in the high-impedance state without an internal pull-up or pull-down, it is recommended to add a pull-up or pull-down resistor or enable the internal pull during software initialization to avoid extra power consumption, selecting the direction as required by the external circuit.
- Avoid using the pins already occupied by flash.
- In Deep-sleep mode, only LP GPIOs can be controlled, which are GPIO0 to GPIO7.

Table 6: IO Pin Default Configuration

No.	Name	Power	At Reset	After Reset
1	ANT			
2	VDDA3			
3	VDDA4			
4	CHIP_PU			
5	XTAL_32K_N/GPIO0	VDDPST_1		
6	XTAL_32K_P/GPIO1	VDDPST_1		
7	GPIO2	VDDPST_1		
8	GPIO3	VDDPST_1		
9	GPIO4	VDDPST_1		
10	GPIO5	VDDPST_1		
11	VDDPST_1			
12	GPIO6	VDDPST_1		
13	GPIO7	VDDPST_1		
14	GPIO8	VDDPST_1		IE
15	GPIO9	VDDPST_1		IE
16	GPIO10	VDDPST_1		IE
17	GPIO11	VDDPST_1		IE
18	VREF_TOUCH			

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Table 6 – continued from previous page

No.	Name	Power	At Reset	After Reset
19	GPIO12	VDDPST_1		IE
20	GPIO13	VDDPST_1		IE
21	GPIO14	VDDPST_1		IE
22	GPIO15	VDDPST_1		IE
23	GPIO16	VDDPST_1		IE
24	GPIO17	VDDPST_1		IE
25	GPIO18	VDDPST_1		IE
26	GPIO19	VDDPST_1		IE
27	SDIO_DATA0	VDDPST_SD		IE
28	SDIO_DATA1	VDDPST_SD		IE
29	SDIO_DATA2	VDDPST_SD		IE
30	VDD_PSRAM_1P8_1			
31	SDIO_DATA3	VDDPST_SD		IE
32	SDIO_CLK	VDDPST_SD		IE
33	SDIO_CMD	VDDPST_SD		IE
34	VDD_PSRAM_1P8_2			
35	VDD_LDO_1P8			
36	SPICS	VDD_SPI	WPU	WPU, IE
37	SPIQ	VDD_SPI	WPU	WPU, IE
38	SPIWP	VDD_SPI	WPU	WPU, IE
39	VDD_SPI			
40	SPIHD	VDD_SPI	WPU	WPU, IE
41	SPICLK	VDD_SPI	WPU	WPU, IE
42	SPID	VDD_SPI	WPU	WPU, IE
43	VCCA/VDDPST_2			
44	USB_DP	VDDPST_2		
45	USB_DM	VDDPST_2		
46	GPIO33	VDDPST_3	DRV=3	USB_PU, IE, DRV=3
47	GPIO34	VDDPST_3	DRV=3	USB_PU, IE, DRV=3
48	GPIO35	VDDPST_3		IE
49	GPIO36	VDDPST_3	IE	IE
50	GPIO37	VDDPST_3	IE	IE
51	GPIO38	VDDPST_3	IE	IE
52	GPIO39	VDDPST_3	IE	IE
53	GPIO40	VDDPST_3	IE	IE
54	VDDPST_3			
55	GPIO42	VDDPST_3		IE
56	GPIO43	VDDPST_3		IE
57	GPIO44	VDDPST_3		IE
58	GPIO45	VDDPST_3		IE
59	GPIO46	VDDPST_3		IE
60	GPIO47	VDDPST_3		IE
61	GPIO48	VDDPST_3		
62	GPIO49	VDDPST_3		
63	VREF_ADC			
64	VDDPST_4			
65	GPIO50	VDDPST_4		
66	GPIO51	VDDPST_4		
67	GPIO52	VDDPST_4		IE
68	GPIO53	VDDPST_4		IE
69	MTDO	VDDPST_4		IE
70	MTCK	VDDPST_4		IE
71	MTDI	VDDPST_4		IE
72	MTMS	VDDPST_4		IE
73	GPIO58	VDDPST_4		IE

continues on next page

Table 6 – continued from previous page

No.	Name	Power	At Reset	After Reset
74	GPIO59	VDDPST_4		IE
75	GPIO60	VDDPST_4	WPU, IE	WPU, IE
76	GPIO61	VDDPST_4	WPU, IE	WPU, IE
77	VDDA1			
78	XTAL_N			
79	XTAL_P			
80	VDDA2			
81	GND			

- IE –input enabled
- WPU –internal weak pull-up resistor enabled
- DRV –drive strength
  - Values 0 ~ 3 correspond to approximately 5, 10, 20, and 40 mA respectively.
  - The default drive current of GPIO33 and GPIO34 is 40 mA. The default drive current of all other IO pins is 20 mA.
- USB_PU –USB pull-up resistor enabled
  - USB pins (GPIO33 and GPIO34) are configured for the USB function by default. Whether these pins are pulled up is determined by the USB pull-up resistor. The USB pull-up is controlled by USB_SERIAL_JTAG_DP/DM_PULLUP, and the USB pull-up resistor value can be controlled through the USB_SERIAL_JTAG_PULLUP_VALUE bit.
  - When the USB function is disabled, the USB pins are used as regular GPIOs, with their internal weak pull-up and pull-down resistors disabled by default. They can be configured through IO_MUX_GPIOn_MCU_WPU/WPD.

1.3.12 ADC

Table below shows the correspondence between ADC channels and GPIOs.

Table 7: ADC Functions

GPIO Pin	ADC Function
GPIO42	ADC1_CH0_N
GPIO43	ADC1_CH0_P
GPIO44	ADC1_CH1_N
GPIO45	ADC1_CH1_P
GPIO46	ADC1_CH2_N
GPIO47	ADC1_CH2_P
GPIO48	ADC1_CH3_N
GPIO49	ADC1_CH3_P
GPIO50	ADC2_CH0_N
GPIO51	ADC2_CH0_P
GPIO52	ADC2_CH1_N
GPIO53	ADC2_CH1_P
MTDO/GPIO54	ADC2_CH2_N
MTCK/GPIO55	ADC2_CH2_P
MTDI/GPIO56	ADC2_CH3_N
MTMS/GPIO57	ADC2_CH3_P

Please add a 0.1 µF filter capacitor between ESP pins and ground when using the ADC function to improve accuracy.

1.3.13 SD/MMC Host Controller

ESP32-S31 series chips integrate one SD/SDIO/MMC host controller (cannot be used as a slave). The SD/MMC host peripheral has two slots that can be used to insert SD cards, connect SDIO devices, or connect eMMC chips. Each slot can be used independently.

- Slot 1 (SDMMC_HOST_SLOT_0) signals are routed via IO MUX using GPIO20 ~ GPIO25, and support SD 3.0 with 1.8 V/3.3 V automatic switching inside the chip.
- Slot 2 (SDMMC_HOST_SLOT_1) signals are routed via IO MUX using GPIO35 ~ GPIO40.

Table 8: SD/MMC GPIO Definition

	DATA0	DATA1	DATA2	DATA3	CLK	CMD
SLOT0	GPIO20	GPIO21	GPIO22	GPIO23	GPIO24	GPIO25
SLOT1	GPIO35	GPIO36	GPIO37	GPIO38	GPIO39	GPIO40

When using slot0, the GPIO power domain is internally powered, so external pull-up resistors are not required. It is recommended to place a series resistor on each signal line and reserve a capacitor to ground on the CLK line for potential debugging and signal tuning. In addition, if 1-bit mode is used, the unused pins must not be repurposed for other functions.

When using slot1, please add pull-up resistors to the GPIO pins. It is also recommended to place a series resistor on each signal line and reserve a capacitor to ground on the CLK line for potential debugging and signal tuning.

1.3.14 USB

ESP32-S31 has a USB 2.0 High-Speed OTG peripheral with integrated transceivers. Pin 44 USB_DP and pin 45 USB_DM serve as the dedicated digital pins for USB_D- and USB_D+ of the USB 2.0 High-Speed OTG interface respectively. Other signals can be routed to any GPIO via the GPIO Matrix.

ESP32-S31 integrates a USB Serial/JTAG controller. GPIO33 and GPIO34 serve as the dedicated digital pins for USB_D- and USB_D+ of the USB Serial/JTAG controller interface respectively.

It is recommended to reserve series resistors (initial value can be 22/33 Ω) and capacitors to ground on the GPIO33 and GPIO34 traces (initially can be unpopulated), and place them close to the chip.

The USB RC circuit is shown in Figure *ESP32-S31 USB RC Schematic*.

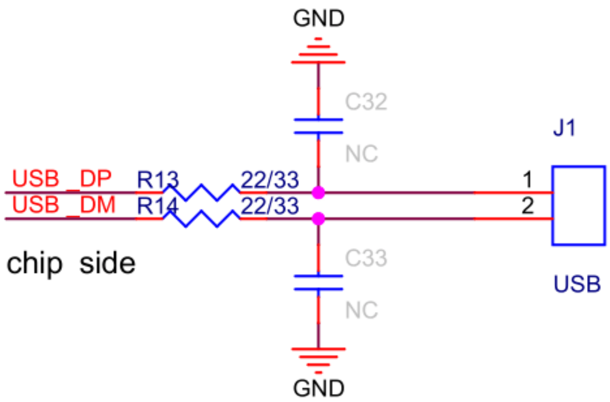

Fig. 11: ESP32-S31 USB RC Schematic

ESP32-S31 also supports download functions and log message printing via USB. For details please refer to Section *Download Guidelines*.

1.3.15 Touch Sensor

ESP32-S31 has 14 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected.

The touch sensing performance is further enhanced by the waterproof design, frequency hopping detection, and digital filtering feature.

Table below shows the correspondence between touch sensor channels and GPIOs.

Table 9: Touch Sensor Functions

GPIO Pin	Touch Sensor Function
GPIO6	TOUCH_CH0
GPIO7	TOUCH_CH1
GPIO8	TOUCH_CH2
GPIO9	TOUCH_CH3
GPIO10	TOUCH_CH4
GPIO11	TOUCH_CH5
GPIO12	TOUCH_CH6
GPIO13	TOUCH_CH7
GPIO14	TOUCH_CH8
GPIO15	TOUCH_CH9
GPIO16	TOUCH_CH10
GPIO17	TOUCH_CH11
GPIO18	TOUCH_CH12
GPIO19	TOUCH_CH13

When using the touch function, it is recommended to populate a series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 kΩ, preferably 510 Ω. The specific value depends on the actual test results of the product.

1.3.16 Ethernet MAC

ESP32-S31 provides an IEEE-802.3 compliant Media Access Controller (MAC) interface for Ethernet communication. It supports communication with an external fast Ethernet PHY through the MII, RMII, or RGMII interface (only one interface can be used at a time).

The interface definitions and the corresponding GPIOs are listed below:

Table 10: EMAC GPIO Definition

GPIO Pin	MII Interface Pin	RMII Interface Pin	RGMII Interface Pin
GPIO8	MII_TXD0	RMII_TXD0	RGMII_TXD0
GPIO9	MII_TXD1	RMII_TXD1	RGMII_TXD1
GPIO10	MII_TXD2	N/A	RGMII_TXD2
GPIO11	MII_TXD3	N/A	RGMII_TXD3
GPIO12	MII_TXEN	RMII_TXEN	RGMII_TX_CTL
GPIO13	MII_TX_CLK	RMII_CLK	RGMII_TX_CLK
GPIO14	MII_RX_CLK	N/A	RGMII_RX_CLK
GPIO15	MII_RXDV	RMII_CRS_DV	RGMII_RX_CTL
GPIO16	MII_RXD3	N/A	RGMII_RXD3
GPIO17	MII_RXD2	N/A	RGMII_RXD2
GPIO18	MII_RXD1	RMII_RXD1	RGMII_RXD1
GPIO19	MII_RXD0	RMII_RXD0	RGMII_RXD0
Any GPIO	MII_RX_ER	N/A	N/A
Any GPIO	MII_CRS	N/A	N/A
Any GPIO	MII_COL	N/A	N/A
Any GPIO	MDIO	MDIO	MDIO
Any GPIO	MDC	MDC	MDC

- It is recommended to add a series resistor on the MII/RMII/RGMII CLK line for tuning.
- The clock signal on the RMII interface (GPIO13) is input only. If a clock output scheme is needed, please use the REF_GMAC_CLK_PAD signal (GPIO35) and connect it to GPIO13 and the PHY side.

1.3.17 LCD and Camera Controller

The ESP32-S31 LCD_CAM controller contains a separate LCD control module and a Camera control module. It can connect to external LCD and camera devices.

The LCD and CAM interfaces of the LCD_CAM controller can be configured to use any GPIO pin via the GPIO matrix. For high-speed requirements, please use the GPIOs defined in the IO MUX, as shown in the table below.

Table 11: LCD IO MUX Interface Definition

GPIO Pin	Parallel LCD Interface Pin	RGB 888 Interface Pin	RGB565 Interface Pin
GPIO2	LCD_DATA19	R3	–
GPIO3	LCD_DATA20	R4	–
GPIO4	LCD_DATA21	R5	–
GPIO5	LCD_DATA22	R6	–
GPIO7	LCD_DATA23	R7	–
GPIO8	LCD_DATA0	B0	B3
GPIO9	LCD_DATA1	B1	B4
GPIO10	LCD_DATA2	B2	B5
GPIO11	LCD_DATA3	B3	B6
GPIO12	LCD_DATA4	B4	B7
GPIO13	LCD_DATA5	B5	G2
GPIO14	LCD_DATA6	B6	G3
GPIO15	LCD_DATA7	B7	G4
GPIO16	LCD_DATA8	G0	G5
GPIO17	LCD_DATA9	G1	G6
GPIO18	LCD_DATA10	G2	G7
GPIO19	LCD_DATA11	G3	R3
GPIO33	LCD_DATA12	G4	R4
GPIO34	LCD_DATA13	G5	R5
GPIO35	LCD_DATA14	G6	R6
GPIO36	LCD_DATA15	G7	R7
GPIO37	LCD_DATA16	R0	–
GPIO38	LCD_DATA17	R1	–
GPIO39	LCD_DATA18	R2	–
GPIO40	LCD_PCLK	LCD_PCLK	LCD_PCLK
GPIO43	LCD_H_ENABLE	LCD_H_ENABLE	LCD_H_ENABLE
GPIO44	LCD_H_SYNC	LCD_H_SYNC	LCD_H_SYNC
GPIO45	LCD_V_SYNC	LCD_V_SYNC	LCD_V_SYNC

Table 12: Camera IO MUX Interface Definition

GPIO Pin	Camera Interface Pin
GPIO46	CAM_DATA0
GPIO47	CAM_DATA1
GPIO48	CAM_DATA2
GPIO49	CAM_DATA3
GPIO50	CAM_DATA4
GPIO51	CAM_DATA5
GPIO52	CAM_DATA6
GPIO53	CAM_DATA7
GPIO54	CAM_PCLK
GPIO55	CAM_XCLK
GPIO56	CAM_V_SYNC
GPIO57	CAM_H_SYNC

1.4 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-S31 PCB layout using an ESP32-S31 module (see Figure *ESP32-S31 Reference PCB Layout*) as an example.

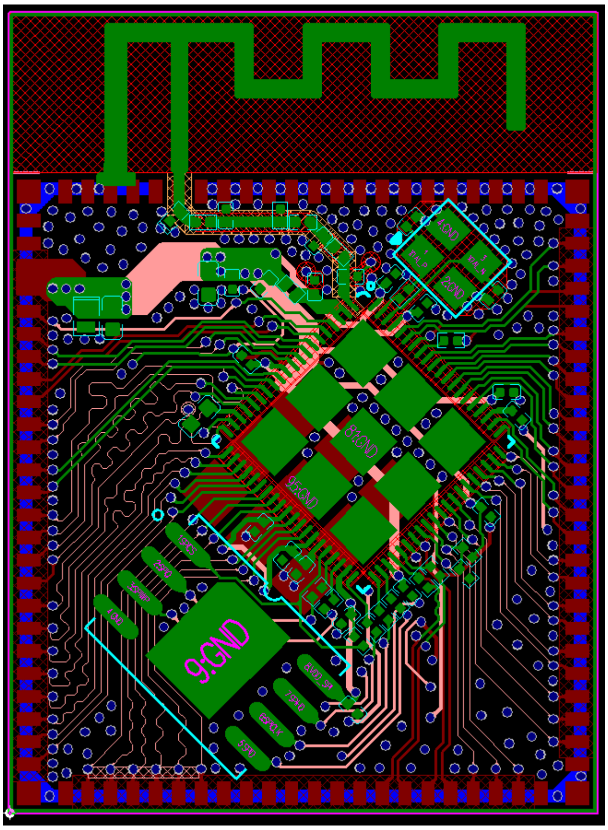

Fig. 12: ESP32-S31 Reference PCB Layout

1.4.1 General Principles of PCB Layout for the Chip

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Apply ground copper. Mainly used for signal traces and components.
- Layer 2 (GND): Apply ground copper. No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): Apply ground copper. Route power traces on this layer. Signal traces are allowed.
- Layer 4 (BOTTOM): Apply ground copper. Signal traces are allowed.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Apply ground copper. Mainly used for components and routing.
- Layer 2 (BOTTOM): Apply ground copper. Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

1.4.2 Power Supply

Four-Layer PCB Design

Figure *ESP32-S31 Power Traces in a Four-Layer PCB Design* shows the power traces in a four-layer PCB design.

- A four-layer PCB design is recommended. Whenever possible, route the power traces on the inner layers (not the ground layer) and connect them to the chip pins through vias. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The yellow highlighted traces in Figure *ESP32-S31 Power Traces in a Four-Layer PCB Design* are all power traces of the chip. The width of the main power traces should be no less than 30 mil. The width of VDDA3

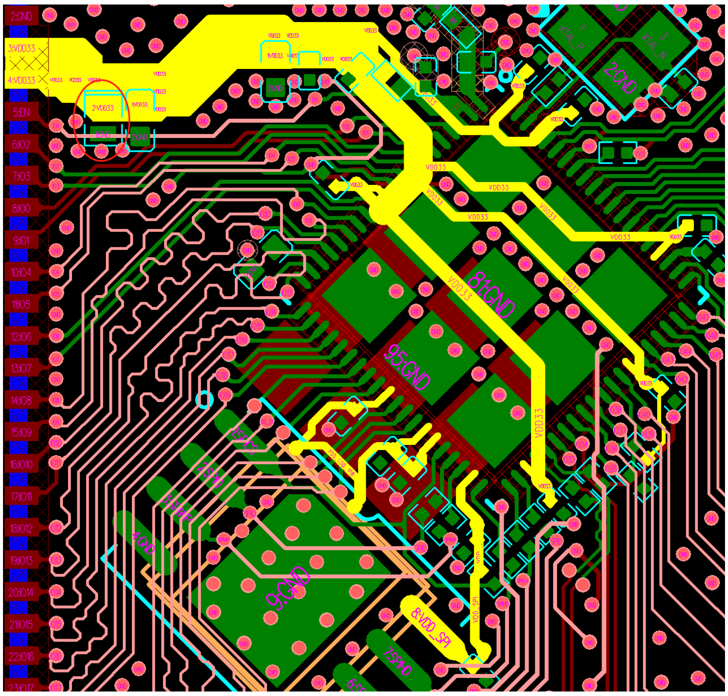

Fig. 13: ESP32-S31 Power Traces in a Four-Layer PCB Design

and VDDA4 power traces should be no less than 20 mil. The recommended width of other power traces is 10 mil. Ensure the power traces are surrounded by ground copper.

- The red circles in *ESP32-S31 Power Traces in a Four-Layer PCB Design* show ESD protection diodes. Place them close to the power input. Add a 10 µF capacitor before the power trace enters the chip. You can also add a 0.1 µF or 1 µF capacitor in parallel. After that, the power trace can branch out in a star-shaped layout to reduce coupling between different power pins.
- The power supply for pin2 and pin3 is RF related, so please place a 10 µF capacitor for each pin. You can also add a 0.1 µF or 1 µF capacitor in parallel.
- Add a CLC/LC filter circuit near pin2 and pin3 to suppress high-frequency harmonics. The power trace can be routed at a 45-degree angle to maintain distance from adjacent RF traces. Except for the 10 µF capacitor, it is recommended to use 0201 components. This allows the filter circuit for pin2 and pin3 to be placed closer to the pins, with a GND isolation layer separating them from surrounding RF and GPIO traces, while also maximizing the placement of ground vias. Using 0201 components enables adding a stub at the first capacitor near the chip to suppress harmonic interference. The stub should reference the bottom layer, with keep-out areas on the other three layers. See Figure *ESP32-S31 Power Traces for Pins 2 and 3*.

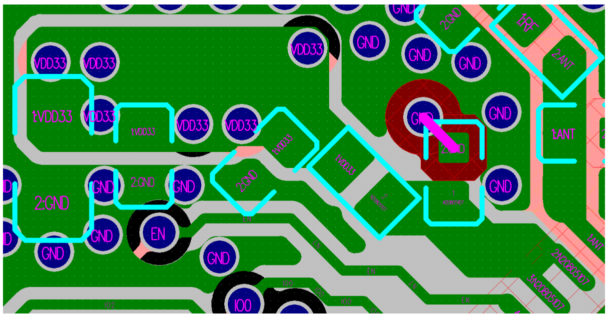

Fig. 14: ESP32-S31 Power Traces for Pins 2 and 3

- Place appropriate decoupling capacitors at the rest of the power pins. Ground vias should be added close to the capacitor's ground pad to ensure a short return path.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground

vias.

- The ground pads of the chip and surrounding circuit components should make full contact with the ground copper pour rather than being connected via traces.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure *ESP32-S31 Power Traces in a Four-Layer PCB Design*. This helps effectively reduce solder leakage issues when soldering the module EPAD to the substrate.

1.4.3 Crystal

Figure *ESP32-S31 Crystal Layout (with Keep-out Area on Top Layer)* shows a reference PCB layout where the crystal is connected to the ground through vias and a keep-out area is maintained around the crystal on the top layer for ground isolation.

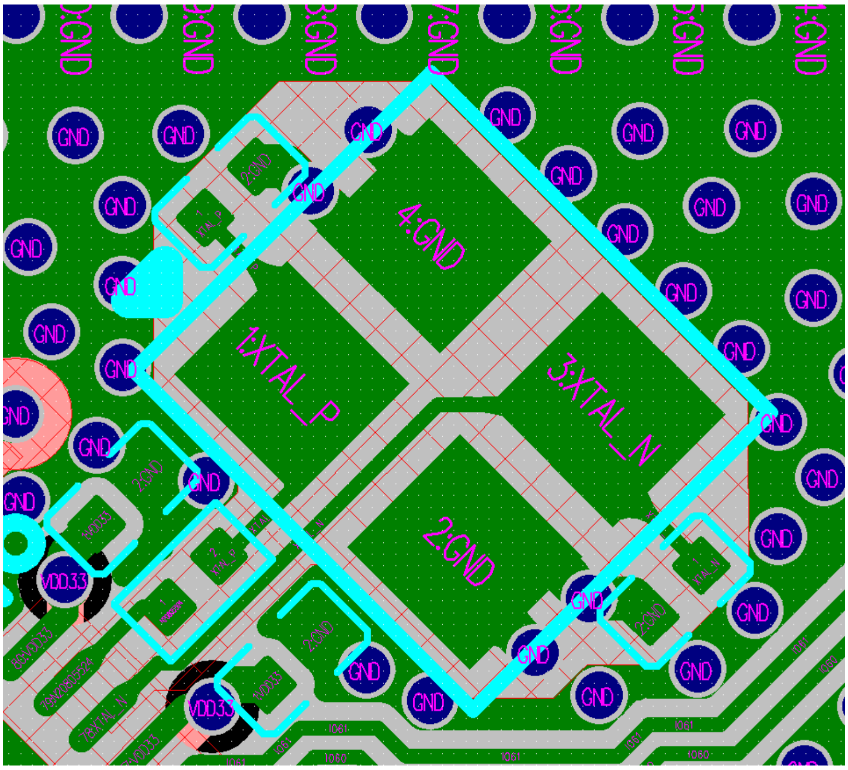

Fig. 15: ESP32-S31 Crystal Layout (with Keep-out Area on Top Layer)

If there is sufficient ground on the top layer, it is recommended to maintain a keep-out area around the crystal for ground isolation. This helps to reduce the value of parasitic capacitance and suppress temperature conduction, which can otherwise affect the frequency offset. If there is no sufficient ground, do not maintain any keep-out area.

The layout of the crystal should follow the guidelines below:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 1.7 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces.
- Components in series to the crystal trace should be placed close to the chip side.
- The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by ground copper.

- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

1.4.4 RF

The RF trace is routed as shown highlighted in pink in Figure *ESP32-S31 RF Layout in a Four-layer PCB Design*.

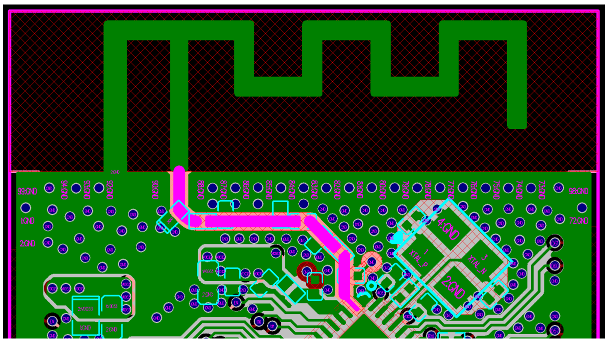

Fig. 16: ESP32-S31 RF Layout in a Four-layer PCB Design

The RF layout should meet the following guidelines:

- The RF trace should have a 50 Ω characteristic impedance. The reference plane is the third layer. For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown below.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	5	17	5

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
CM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	1080		2.79	4.2
L2_Gnd		1	1.2	
Core	Core		19.69	4.6
L3_Power		1	1.2	
PP	1080		2.79	4.2
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Fig. 17: ESP32-S31 PCB Stack-up Design

> **Attention:** The third layer is used as the reference plane for this module because, with the current stack-up structure, the RF trace width differs too much from the component pad size. To avoid abrupt transitions from the trace to component pads, the area under the RF trace on the second layer is cleared, and the third layer is used as the reference ground plane to obtain RF traces of suitable width.
>
> If the stack-up used does not have this issue, it is recommended to use the layer adjacent to the chip as the reference ground plane.

- A CLCCL matching circuit is required for chip tuning. Please use 0201 components and place them close to the pin in a zigzag. In other words, the two capacitors should not be oriented in the same direction to minimize interference.
- Add a stub on the ground pad of the grounding capacitor near the chip side in the matching circuit to suppress the second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up so that the characteristic impedance of the stub is 100 Ω ± 10%. The reference plane is the third layer, so the area under the trace on the second layer should be cleared. The trace highlighted in Figure *ESP32-S31 Stub in a Four-layer PCB Design* is the stub. Note that a stub is not required for package types of 0402 and above.
- It is recommended to keep all layers clear under the IPEX antenna connector. See Figure *ESP32-S31 IPEX Antenna Connector Layout*.
- For PCB antennas, make sure to validate them through both simulation and real-world testing on a development board. It is recommended to include an additional CLC matching circuit for antenna tuning. Place this circuit as close to the antenna as possible.

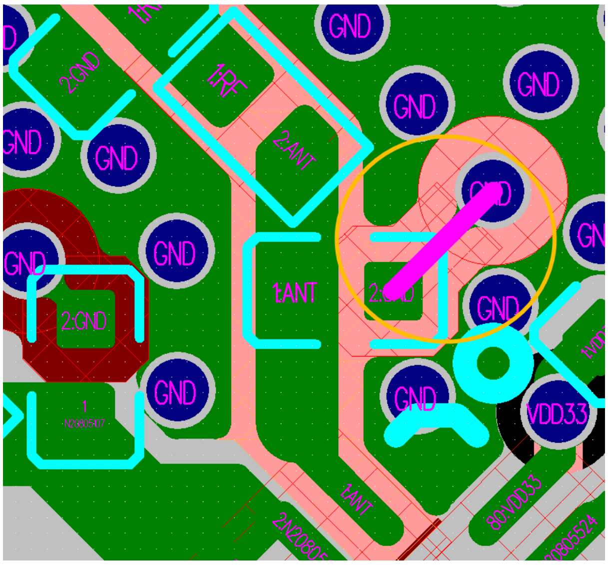

Fig. 18: ESP32-S31 Stub in a Four-layer PCB Design

- The RF trace should have a consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

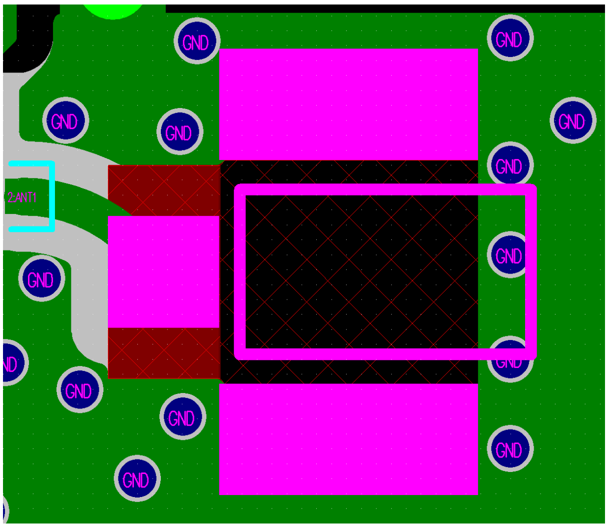

Fig. 19: ESP32-S31 IPEX Antenna Connector Layout

1.4.5 Flash and PSRAM

The layout for flash and PSRAM should follow the guidelines below:

- Place the zero-ohm resistors in series on the SPI lines close to ESP32-S31.
- Route the SPI traces on the inner layer (e.g., the third layer) whenever possible, and add ground copper and ground vias around the clock and data traces of SPI separately.
- If the flash and PSRAM are located far from ESP32-S31, it is recommended to place appropriate decoupling capacitors both at VDD_SPI and near the flash and PSRAM power supply.

Figure *ESP32-S31 Quad SPI Flash Layout* shows the quad SPI flash layout.

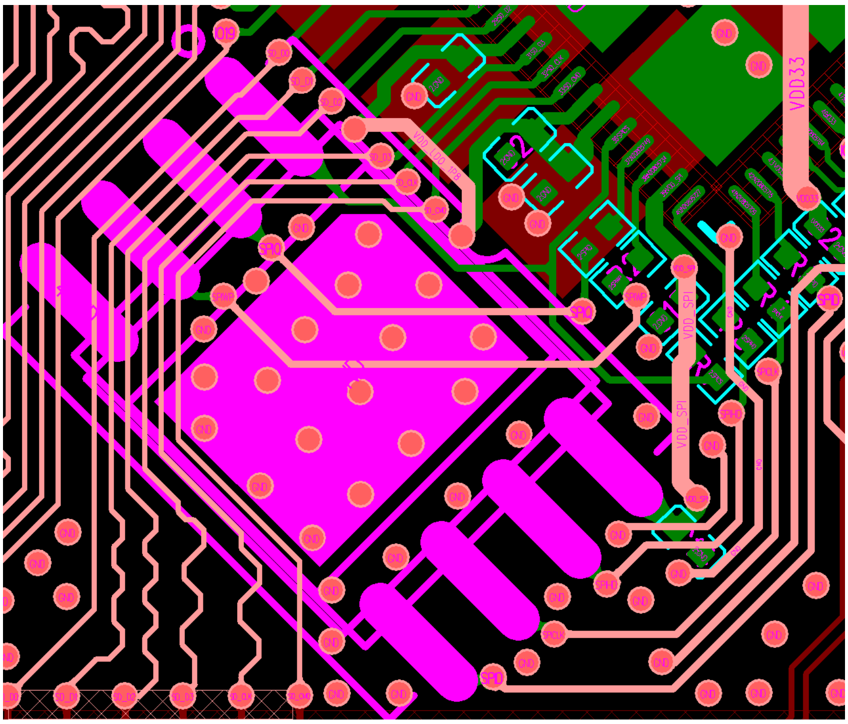

Fig. 20: ESP32-S31 Quad SPI Flash Layout

1.4.6 UART

Figure *ESP32-S31 UART Layout* shows the UART layout.

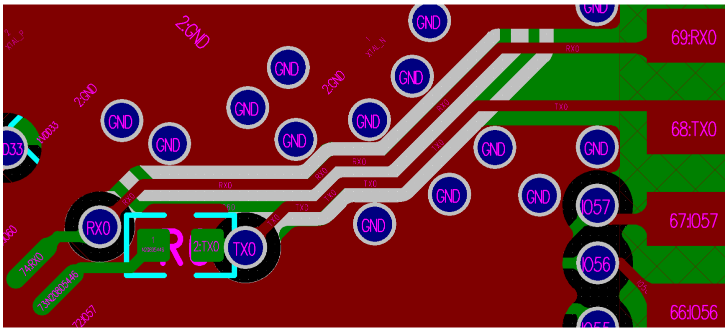

Fig. 21: ESP32-S31 UART Layout

The UART layout should meet the following guidelines:

- The series resistor on the U0TXD trace needs to be placed close to the chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.
- The UART trace should be surrounded by ground copper and ground vias stitching.

1.4.7 General Principles of PCB Layout for Modules (Positioning a Module on a Base Board)

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the baseboard on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna close to the edge of the base board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

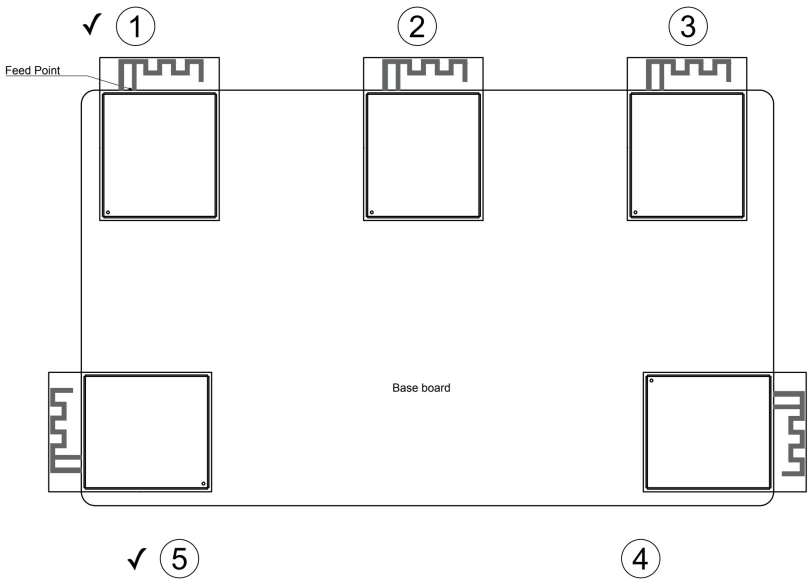

Fig. 22: Placement of ESP32-S31 Modules on Base Board (antenna feed point on the left)

If the antenna cannot extend beyond the board edge, the feed point should still be placed as close to the board edge as possible. Then cut off the base board on both sides of the antenna and below it to minimize the impact of the base board material on the PCB antenna and provide a sufficiently large clearance area for the PCB antenna. Note that the module should not be placed in the center of the board with clearance created by hollowing out on all four sides. Figure *Keepout Zone for ESP32-S31 Module's Antenna (Antenna feed point on the Left)* shows the suggested clearance area. Please note that sufficient ground copper and dense ground vias should be placed on the base board near the antenna.

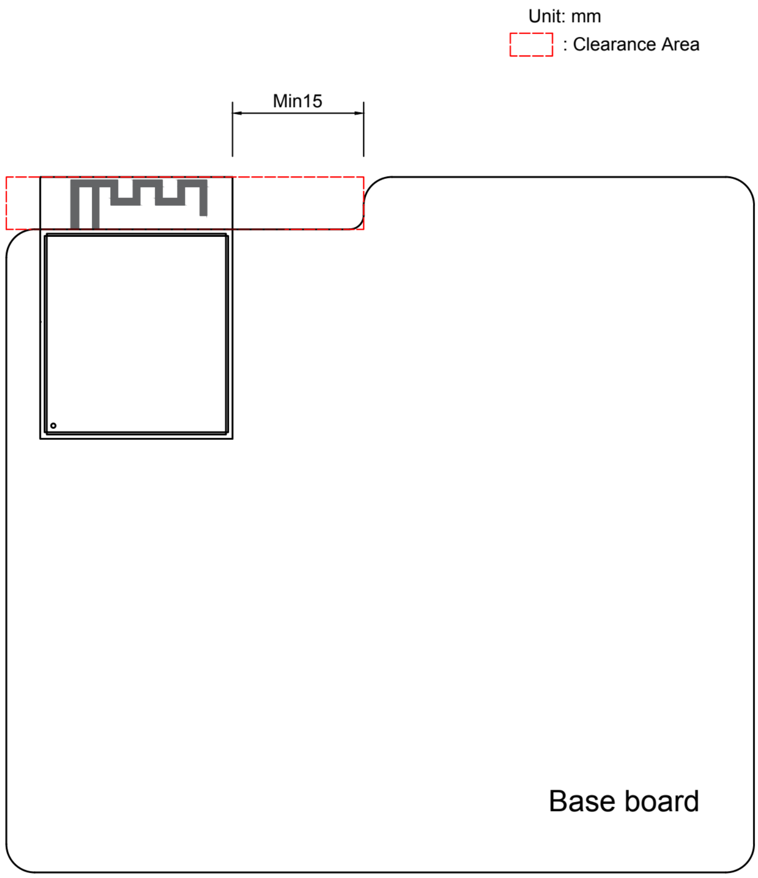

Fig. 23: Keepout Zone for ESP32-S31 Module's Antenna (Antenna feed point on the Left)

After the base board is placed in the end product, please consider the impact of the housing on the antenna during end-product design. Ensure that the PCB antenna on the base board also has a sufficiently large clearance area inside the housing. A clearance of at least 15 mm is recommended in all directions.

Please note that the final end product should be tested for throughput and communication range to ensure RF performance.

1.4.8 ADC

The ADC layout should follow the guidelines below:

- For high-precision ADC, the P and N traces should be routed close together with a spacing of 1~1.5 times the trace width between them. Ensure ground isolation from other traces.

1.4.9 USB

The USB layout should meet the following guidelines:

- Reserve space for resistors and capacitors on the USB traces close to the chip side.
- Use differential pairs and route them in parallel at equal lengths. Maintain a differential pair impedance of 90 Ω with a tolerance of ±10%.
- USB differential traces should minimize via transitions as much as possible to ensure better impedance control and avoid signal reflections. If vias are necessary, add a pair of ground return vias at each transition point.
- Ensure there is a continuous reference layer (a ground layer is recommended) beneath the USB traces.
- Surround the USB traces with ground copper.

1.4.10 SDIO

The SDIO layout should follow the guidelines below:

- Minimize parasitic capacitance of SDIO traces as they involve high-speed signals.
- The trace lengths for SDIO_CMD and SDIO_DATA0 ~ SDIO_DATA3 should be within ± 50 mil of the SDIO_CLK trace length. Use serpentine routing if necessary.
- For SDIO routing, maintain a 50 Ω single-ended impedance with a tolerance of ±10%.
- Keep the total trace length from SDIO GPIOs to the master SDIO interface as short as possible, ideally within 2000 mil.
- Ensure that SDIO traces do not cross layers. Besides, a reference plane (preferably a ground plane) must be placed beneath the traces, and continuity of the reference plane must be ensured.
- It is recommended to surround the SDIO_CLK trace with ground copper.

1.4.11 Touch Sensor

ESP32-S31 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip' s internal capacitance detection circuit features low noise and high sensitivity. It allows to use touch pads with smaller area to implement the touch detection function. You can also use the touch panel array to detect a larger area or more test points.

Figure *ESP32-S31 Typical Touch Sensor Application* depicts a typical touch sensor application.

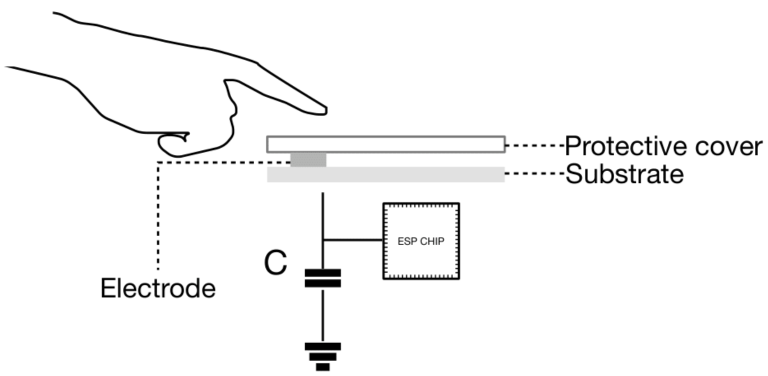

Fig. 24: ESP32-S31 Typical Touch Sensor Application

To prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip are commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

Figure *ESP32-S31 Electrode Pattern Requirements* shows the proper and improper size or shape of electrode. Please note that the examples illustrated in the figure are not of actual scale. It is suggested to use a human fingertip as reference.

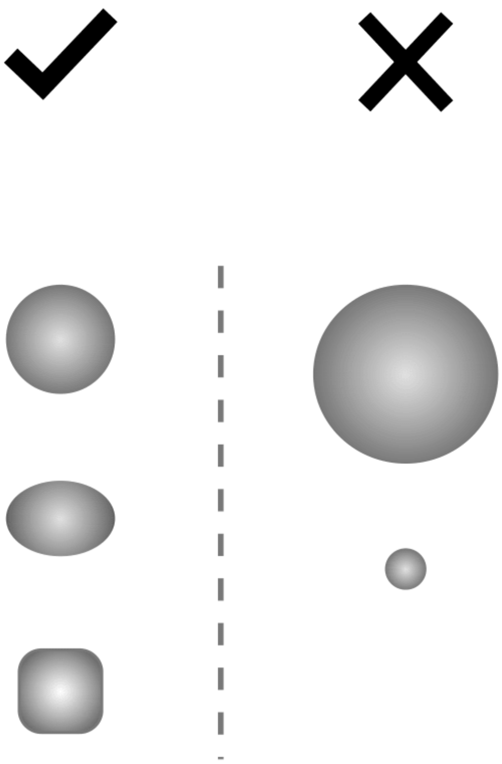

Fig. 25: ESP32-S31 Electrode Pattern Requirements

PCB Layout

Figure *ESP32-S31 Sensor Track Routing Requirements* illustrates the general guidelines to routing traces. Specifically,

- The trace should be as short as possible and no longer than 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.
- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

Note: For more details on the hardware design of the touch sensor, please refer to Touch Sensor Application Note.

Waterproof and Proximity Sensing Design

ESP32-S31 touch sensor has a waterproof design and features proximity sensor function. Figure *ESP32-S31 Waterproof and Proximity Sensing Design* shows an example layout of a waterproof and proximity sensing design.

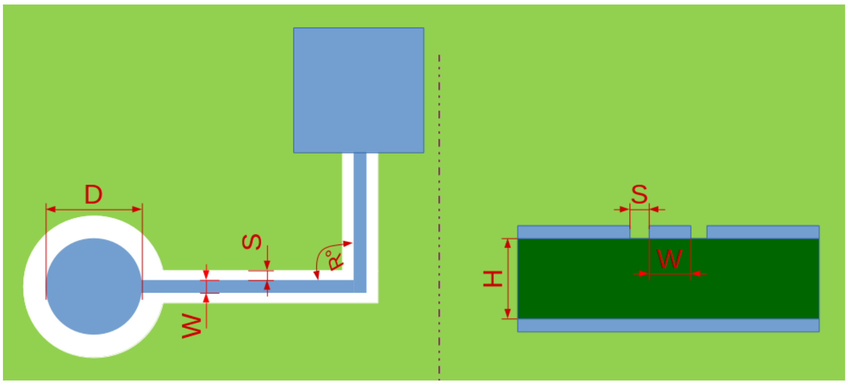

Fig. 26: ESP32-S31 Sensor Track Routing Requirements

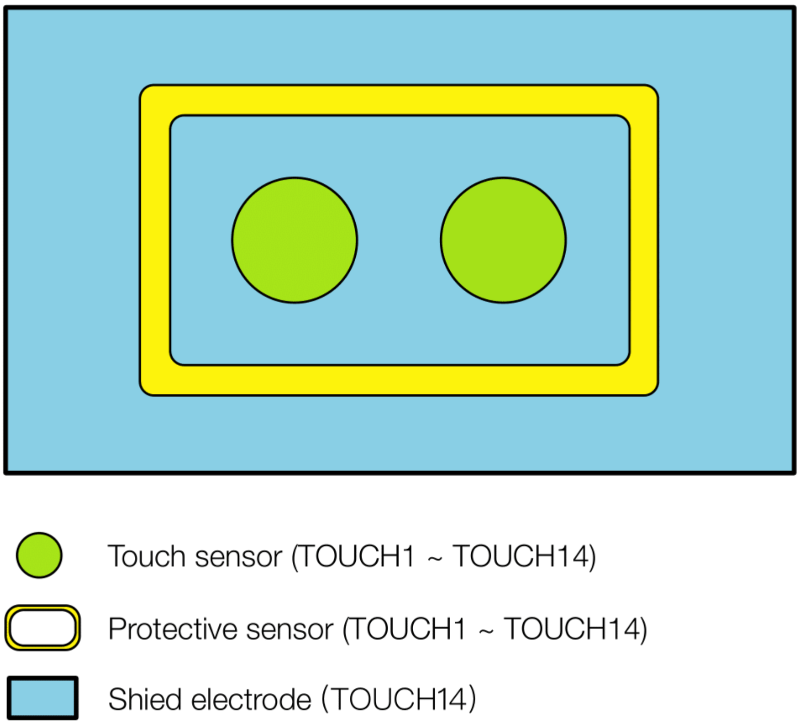

Fig. 27: ESP32-S31 Waterproof and Proximity Sensing Design

Note the following guidelines to better implement the waterproof and proximity sensing design:

- The recommended width of the shield electrode width is 2 cm.
- Employ a grid on the top layer with a trace width of 7 mil and a grid width of 45 mil (25% fill). The filled grid is connected to the driver shield signal.
- Employ a grid on the bottom layer with a trace width of 7 mil and a grid width of 70 mil (17% fill). The filled grid is connected to the driver shield signal.
- The protective sensor should be in a rectangle shape with curved edges and surround all other sensors.
- The recommended width of the protective sensor is 2 mm.
- The recommended gap between the protective sensor and shield sensor is 1 mm.
- The sensing distance of the proximity sensor is directly proportional to the area of the proximity sensor. However, increasing the sensing area will introduce more noise. Actual testing is needed for optimized performance.
- It is recommended that the shape of the proximity sensor is a closed loop. The recommended width is 1.5 mm.

1.4.12 EMAC

The EMAC layout should follow the guidelines below:

- EMAC traces should maintain a 50 Ω single-ended impedance with a tolerance of ±10%.
- EMAC traces should follow the basic 3W rule for high-speed digital circuit routing.
- For the MII/RGMII interface, TX data trace lengths should be within ± 50 mil of the TX_CLK trace length, and RX data trace lengths should be within ± 50 mil of the RX_CLK trace length. Use serpentine routing if necessary.
- A reference layer must be placed beneath EMAC traces, and continuity of the reference layer must be ensured.
- For multi-layer PCB designs, it is recommended to route EMAC traces to the inner layers immediately after exiting the chip through vias, in order to reduce interference on high-speed signal lines. Additionally, place a pair of ground vias near the layer transition to ensure proper return path.
- EMAC traces should be isolated from other traces with ground copper.

1.4.13 Typical Layout Problems and Solutions

When ESP32-S31 sends data packages, the voltage ripple is small, but RF TX performance is poor.

Analysis: The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution: This problem is caused by improper layout for the crystal and can be solved by re-layout. Please refer to Section *Crystal* for details.

When ESP32-S31 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis: The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution: Match the antenna’s impedance with the π-type circuit on the RF trace, so that the impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

TX performance is not bad, but the RX sensitivity is low.

Analysis: Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution: Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please refer to Section *RF* for details.

1.5 Download Guidelines

You can download firmware to ESP32-S31 via UART and USB.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, according to Table *Chip Boot Mode Control*.
2. Power up the chip or module and check the log via the UART0 serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Use the `Flash Download Tool` to flash firmware into flash via UART.
4. After the firmware has been downloaded, configure the chip to work in SPI Boot mode according to Table *Chip Boot Mode Control*.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. If the flash is empty, set the chip or module to Joint Download Boot mode, according to Table *Chip Boot Mode Control*.
2. Power up the chip or module and check the log via USB serial port. If the log shows "waiting for download", the chip or module has entered Joint Download Boot mode.
3. Use the `Flash Download Tool` to flash firmware into flash via USB.
4. After the firmware has been downloaded, configure the chip to work in SPI Boot mode according to Table *Chip Boot Mode Control*.
5. Power up the chip or module again. The chip will read and execute the new firmware during initialization.
6. If the flash is not empty, start directly from Step 3.

Note:

- For firmware download instructions, see also ESP Product Firmware Download Instructions.
- For how to check serial port output, see also Establish Serial Connection with ESP32-S31.
- It is advised to download the firmware only after the "waiting for download" log shows via the serial port.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one COM port.

- The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip or module to Joint Download Boot mode first by configuring the strapping pin.
  - USB PHY is disabled by the application;
  - USB is configured for other USB functions, e.g., USB host, USB standard device;
  - USB IOs are configured to other peripherals, such as UART and LEDC.
- It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.
- It is recommended to retain the UART download interface, as the current RF test firmware only supports the UART interface.

1.6 Related Documentation and Resources

1.6.1 ESP32-S31 Modules

For a list of ESP32-S31 modules please check the Modules section on Espressif's official website.

1.6.2 ESP32-S31 Development Boards

For a list of the latest designs of ESP32-S31 boards please check the Development Boards section on Espressif's official website.

1.6.3 Other Related Documentation and Resources

- Chip Datasheet (PDF)
- ESP32-S31 Chip Variants
- Espressif KiCad Library
- ESP Product Selector
- Regulatory Certificates
- User Forum (Hardware)
- Technical Support
- ESP-FAQ

1.7 Glossary

The glossary contains terms and acronyms that are used in this document.

Term	Description
CLC	Capacitor-Inductor-Capacitor
DDR SDRAM	Double Data Rate Synchronous Dynamic Random-Access Memory
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
Zero-ohm resistor	A zero-ohm resistor acts as a placeholder in the circuit, allowing for the replacement with a higher-ohm resistor based on specific design requirements.

1.8 Revision History

Table 13: Revision History

Date	Version	Release Notes
2026-06-23	v0.1	First release

1.9 Disclaimer and Copyright Notice