GC9503NP

a-Si TFT LCD Single-Chip Driver
480(RGB)x960 Resolution, 16.7M-color
Without internal GRAM

Datasheet

V1.7

2021-02-02

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2017-10-12	Document Release	June
V1.1	2017-11-27	Resolution 480RGB*960	June
V1.2	2018-1-9	Page0 Reg, IC Top View Updata	June
V1.3	2018-3-23	DCC Review	Flower
V1.4	2018-6-6	Temperature	June
V1.5	2018-6-8	Pad change	June
V1.6	2020-12-30	AE Review	Evie
V1.7	2021-2-2	Temperature	Evie

Table of Content

1 DESCRIPTION

The GC9503NP device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 480RGBx960, 480RGBx864, 480RGBx854, 480RGBx800, 480RGBx720, 480RGBx640, 480RGBx360 without internal GRAM. It includes a timing controller with glass interface level-shifters and a glass power supply circuit.

The GC9503NP supports MIPI Interface, 16/18/24 bits RGB interface, serial peripheral interfaces (SPI) interface. The GC9503NP is also able to make gamma correction settings separately for RGB dots to panel characteristics, resulting in higher display qualities.

This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA.

2 FEATURES

Display resolution option
- 480RGB x 960
- 480RGB x 864
- 480RGB x 854
- 480RGB x 800
- 480RGB x 720
- 480RGB x 640
- 480RGB x 360

Display mode (Color mode)
- Full color mode: 16.7M-colors
- Reduce color mode: 262K colors
- Reduce color mode: 65K colors
- Idle mode: 8 colors

Interface
- 8-bit, 9-bit and 16-bit serial peripheral interface
- 16-/18-/24-bits RGB interface (DE mode and SYNC mode with polarity of HS/VS can be set by register)
- MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
  Supports one data lanes / maximum speed 500Mbps
  Supports two data lanes / maximum speed 500Mbps

Display features
- Individual gamma correction setting for RGB dots
- Deep standby function

On chip Build-In Circuits
- DC/DC Conveter
- VGHO/VGLO voltage generator for gate control signal and panel
- Oscillator for display clock
- Supports gate control signals to gate driver in the panel

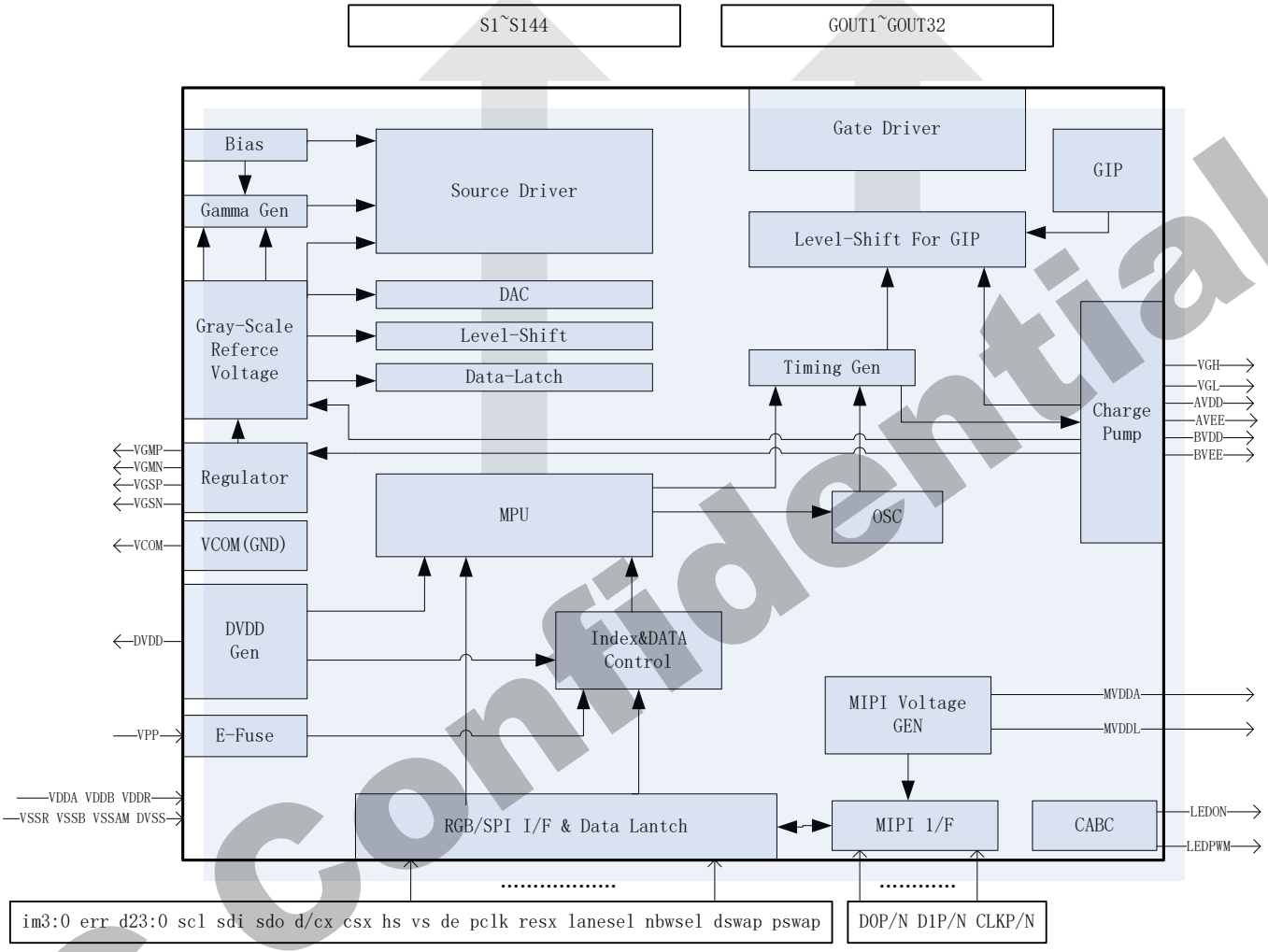
Driving Algorithm Support
- Column Inversion
- Dot Inversion

Supply voltage range
- I/O supply voltage range for VDDI to GND: 1.65V ~ 3.3V
- Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR: 2.5V ~ 3.3V

On-Chip Power System
- Positive gate driver voltage range for VGH: 9.0 ~ 16V
- Negative gate driver voltage range for VGL: -8.0~ -12V
- Step-up 1 output voltage range for AVDD/BVDD: 6.0 ~ 7.0V
- Step-up 2 output voltage range for AVEE/BVEE: -4.2 ~ -5.2V
- Positive gamma high voltage range for VGMP: 4.5 ~ 6.5V (AVDD-0.5V)
- Positive gamma low voltage range for VGSP: 0.7 ~ 1.8V
- Negative gamma high voltage range for VGMN: -4.5~ -2.5V (AVEE+0.5V)
- Negative gamma low voltage range for VGSN: 0.7 ~ 1.8V
- Common electrode voltage range for VCOM: GND Level

Operate temperature range: −40℃ to +85℃

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

4.1 PIN DESCRIPTION

<table>
<tr><th colspan="3">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>-Select the interface mode
Interface type selection. The connections of IM[3:0] which not shown in table are invalid.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8-bit spi(scl rising edge</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8-bit spi(scl falling edge</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>9-bit spi(scl rising edge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>9-bit spi(scl falling edge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>16-bit spi(scl rising edge</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>16-bit spi(scl falling edge</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="2">MIPI DSI, D0_P/N, D1_P/N</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>-A chip select signal.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to VDDI level when not in use.</td></tr>
<tr><td>SCL</td><td>I</td><td>- The SPI Interface (SCL): Serves as a write signal and writes data at the rising edge.
- Serial interface (SCL): Serial clock input.
Fix to VDDI level when not in use.</td></tr>
<tr><td>D/CX</td><td>I</td><td>-Display data/command selection in 8-bit SPI I/F
D/CX = “0”:command
D/CX = “1”:parameter
Fix to VDDI level when not in use.</td></tr>
<tr><td>DB[23:0]</td><td>I/O</td><td>- A 24-bit parallel bi-directional data bus for DPI (RGB) I/F</td></tr>
</table>

<table>
<tr><td></td><td></td><td>Fix to DGND level when not in use</td></tr>
<tr><td>SDI</td><td>I</td><td>-Serial data input pin used for the SPI Interface. SDI : Serial data input pin
Fix to VDDI level when not in use</td></tr>
<tr><td>SDO</td><td>O</td><td>-Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together.
please open this pin when not in use</td></tr>
<tr><td>PCLK</td><td>I</td><td>- Dot clock signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>VS</td><td>I</td><td>- Frame synchronizing signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>HS</td><td>I</td><td>- Line synchronizing signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>DE</td><td>I</td><td>- Data enable signal for DPI (RGB) interface operation.
Low : access enabled.
High : access inhibited.
Fix to DGND level when not in use.</td></tr>
<tr><td>HS_CP
HS_CN</td><td>I</td><td>MIPI DSI differential clock pair (DSI-CLK+/-).
If MIPI are not used, they should be connected to DGND.</td></tr>
<tr><td>HS_D0P
HS_D0N
HS_D1P
HS_D1N</td><td>I/O</td><td>MIPI DSI differential data pair (DSI-Dn+/-).
If MIPI are not used, they should be connected to DGND</td></tr>
<tr><td>ERR</td><td>O</td><td>- CRC and ECC error output pin for MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found.
Leave the pin to open when not in use.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>- Input pin to select 1 data lane or 2 data lanes in MIPI interface.
Low: 1 data lane. High: 2 data lanes.
- The pin have internal pull low resister.
Fix to DGND level when not in use.</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>- Differential clock polarity swap
For MIPI DSI interface
<table>
<tr><th colspan="2">Pin Name</th><th>HS_D0P</th><th>HS_D0N</th><th>HS_CP</th><th>HS_CN</th><th>HS_D1P</th><th>HS_D1N</th></tr>
<tr><td>Input</td><td>DSWAP=0
PSWA</td><td>DSI-D0+</td><td>DSI-D0-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D1+</td><td>DSI-D1-</td></tr>
</table></td></tr>
</table>

		MIPI Signal P=0 DSWAP=0 PSWAP=1: DSI-D0-, DSI-D0+, DSI-CLK-, DSI-CLK+, DSI-D1-, DSI-D1+ DSWAP=1 PSWAP=0: DSI-D1+, DSI-D1-, DSI-CLK+, DSI-CLK-, DSI-D0+, DSI-D0- DSWAP=1 PSWAP=1: DSI-D1-, DSI-D1+, DSI-CLK-, DSI-CLK+, DSI-D0-, DSI-D0+ Fix to DGND level when not in use.
NBWSEL	I	- Input pin to select the gamma voltage level sequence of V0~V255. Low: V0>V1>…>V254>V255, normally white. High: V255>V254>…>V1>V0, normally black. Fix to DGND level when not in use.
LEDON	O	- Used for turning On/Off external LED backlight control. Leave the pin to open when not in use.
LEDPWM	O	- The PWM frequency output for LED driver control. Leave the pin to open when not in use.

Driver Output		
Pin Name	**I/O**	**Description**
S[1:1440]	O	- Source output voltage signals applied to a LCD panel.
GOUT[1:32]	O	- Gate control signals and the swing voltage level is VGHO to VGLO.
GOUT_VGHO	O	- High voltage level for GIP control signals and gate circuit of panel.
GOUT_VGLO	O	- Low voltage level for GIP control signals and gate circuit of panel.
VGHO	O	- High voltage level for GIP control signals and gate circuit of panel.
VGLO	O	- Low voltage level for GIP control signals and gate circuit of panel.
LVGL	O	- Low voltage level for gate circuit of panel.
VCOM	O	- Fix GND

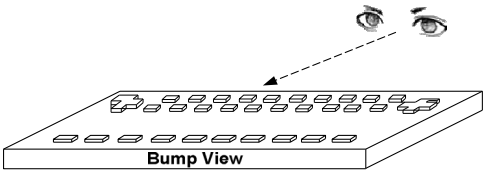
Charge Pump Pin		
Pin Name	**I/O**	**Description**
BVDD	O	OPEN

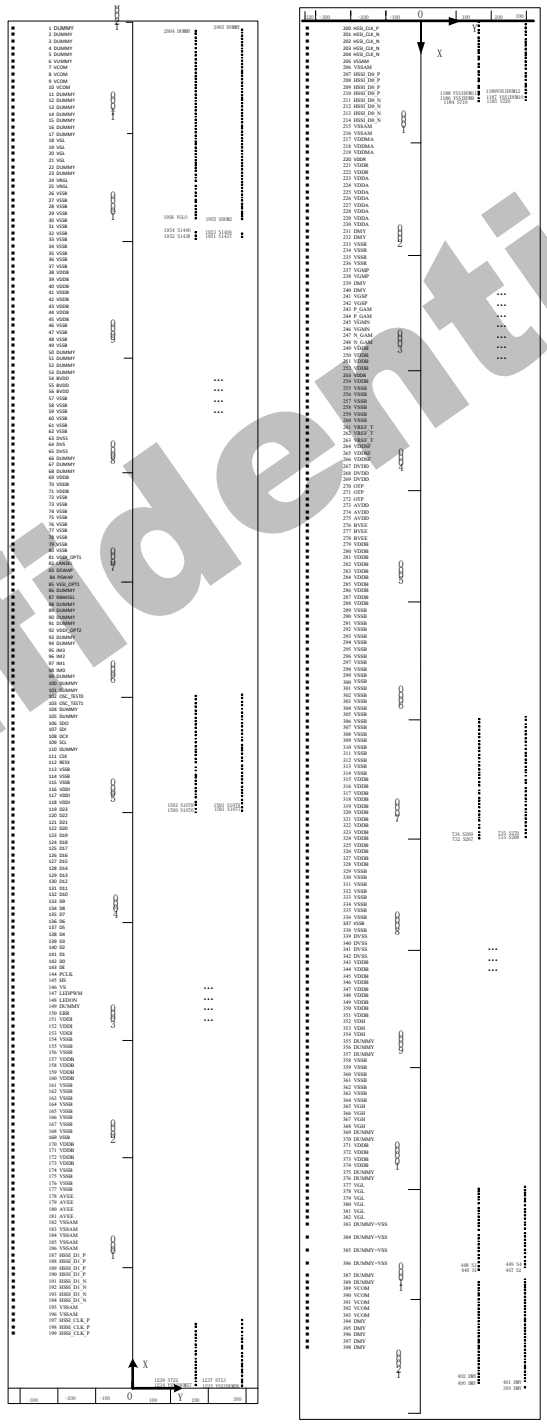
BVEE	O	OPEN
AVDD	O	OPEN
AVEE	O	OPEN
VGH	O	OPEN
VGL	O	OPEN

Power Pin		
Pin Name	**I/O**	**Description**
VDDA	P	- Power supply for analog system. - VDDA,VDDB and VDDR should be the same input voltage level of 2.5 ~ 3.3V.
VDDR	P	- Power supply for regulator low voltage reference circuit. - VDDA,VDDB and VDDR should be the same input voltage level of 2.5 ~ 3.3V.
VDDB	P	- Power supply for DC/DC converter. - VDDA,VDDB and VDDR should be the same input voltage level of 2.5 ~ 3.3V.
VDDI	P	- Power supply for I/O block. ***Excluded MIPI interface.***
DVDD	O	- internal logic voltage output
VGH_REG	O	- Output voltage generated from VGH. ***Leave the pin to open when not in use.***
VGL_REG	O	- Output voltage generated from VGL. LDO output used for panel voltage. ***Leave the pin to open when not in use.***
VGMP/VGSP	O	- Output voltage generated from DDVDH. LDO output for positive gamma voltage generator.
VGMN/VGSN	O	- Output voltage generated from DDVDL. LDO output for negative gamma voltage generator.
MVDDA	O	- Regulator output for internal MIPI DSI analog system (1.5V typical)
MVDDL	O	- Regulator output for internal MIPI DSI low power system (1.2V typical)
VSSA	P	- System ground for analog circuit.
VSSAM		- System ground for MIPI circuit.
VSSR		- System ground for internal digital system.
VSSB	P	- System ground for DC/DC convertor.
DVSS	P	- System ground for Digital circuit.
VPP	I	- OTP programming power.

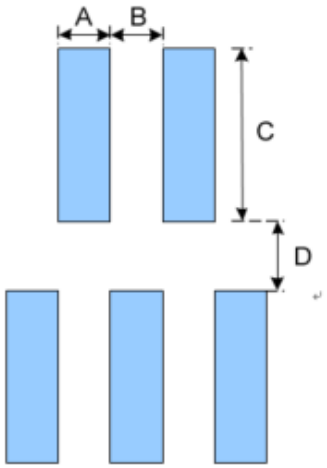
4.2 Output Bump Dimension

Gate : GO1~GO32
Source : S1~S1440
Input Pads : Pad 1 to Pad 398



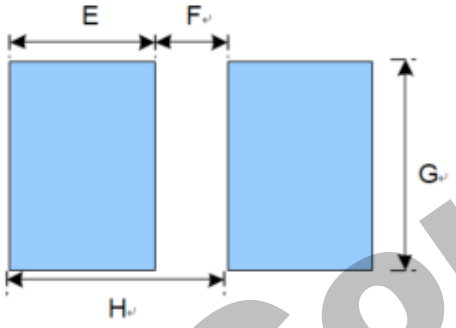


4.3 Input Bump Dimension



Input Pads

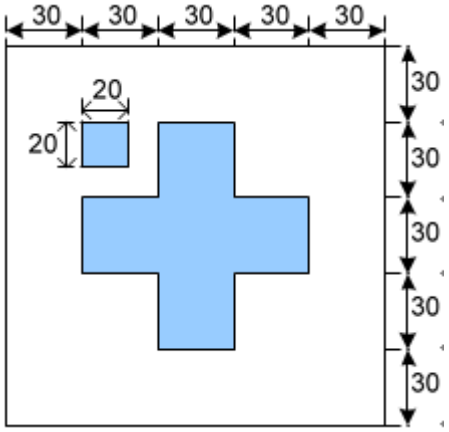
Symbol	Item	Size
A	Bump Width	13 um
B	Bump Gap 1 (Horizontal)	15 um
C	Bump Height	81 um
D	Bump Gap 2 (Vertical)	47 um



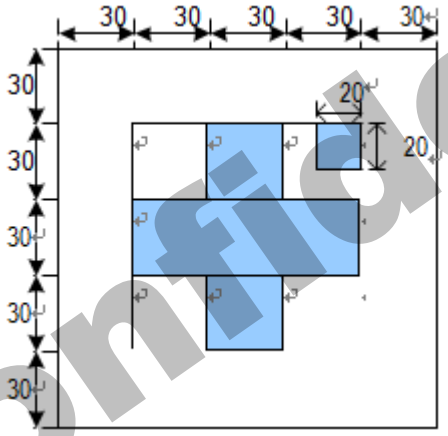
Output Pads

Symbol	Item	Size
E	Bump Width	40 um
F	Bump Gap	20um
G	Bump Height	51um
H	Bump Pitch	60 um
	Bump thickness	9um

4.4 Alignment Mark Dimension



- Alignment Mark ALIGN_L : (X,Y)=(-11870,287.5)



- Alignment Mark ALIGN_R : (X,Y)=(+11870,287.5)

4.5 Chip Information

Chip size	24720μm x690μm(not include scribe line)
Chip thickness	250um
Pad Location	Pad center
Coordinate Origin	Chip center

4.6 Pad Coordination

No	Pad	X	Y
1	DMY	-11910	-313.5
2	DMY	-11850	-313.5
3	DMY	-11790	-313.5
4	DMY	-11730	-313.5
5	DMY	-11670	-313.5
6	VCOM	-11610	-313.5
7	VCOM	-11550	-313.5
8	VCOM	-11490	-313.5
9	VCOM	-11430	-313.5
10	VCOM	-11370	-313.5
11	DMY	-11310	-313.5
12	DMY	-11250	-313.5
13	DUMMY	-11190	-313.5
14	DUMMY	-11130	-313.5
15	DUMMY	-11070	-313.5
16	DUMMY	-11010	-313.5
17	DUMMY	-10950	-313.5
18	VGL	-10890	-313.5
19	VGL	-10830	-313.5
20	VGL	-10770	-313.5
21	VGL	-10710	-313.5
22	DUMMY	-10650	-313.5
23	DUMMY	-10590	-313.5
24	VRGL	-10530	-313.5
25	VRGL	-10470	-313.5
26	VSSB	-10410	-313.5
27	VSSB	-10350	-313.5
28	VSSB	-10296.	-313.5
29	VSSB	-10230	-313.5
30	VSSB	-10170	-313.5
31	VSSB	-10110	-313.5
32	VSSB	-10050	-313.5
33	VSSB	-9990	-313.5
34	VSSB	-9930	-313.5
35	VSSB	-9870	-313.5
36	VSSB	-9810	-313.5
37	VSSB	-9750	-313.5
38	VDDB	-9690	-313.5
39	VDDB	-9630	-313.5
40	VDDB	-9570	-313.5
41	VDDB	-9510	-313.5
42	VDDB	-9450	-313.5
43	VDDB	-9390	-313.5
44	VDDB	-9330	-313.5
45	VDDB	-9270	-313.5
46	VSSB	-9210	-313.5
47	VSSB	-9150	-313.5
48	VSSB	-9090	-313.5
49	VSSB	-9030	-313.5
50	DUMMY	-8970	-313.5

No.	Pad	X	Y
51	DUMMY	-8910	-313.5
52	DUMMY	-8850	-313.5
53	DUMMY	-8790	-313.5
54	BVDD	-8730	-313.5
55	BVDD	-8670	-313.5
56	BVDD	-8610	-313.5
57	VSSB	-8550	-313.5
58	VSSB	-8490	-313.5
59	VSSB	-8430	-313.5
60	VSSB	-8370	-313.5
61	VSSB	-8310	-313.5
62	VSSB	-8250	-313.5
63	DVSS	-8190	-313.5
64	DVSS	-8130	-313.5
65	DVSS	-8070	-313.5
66	DUMMY	-8010	-313.5
67	DUMMY	-7950	-313.5
68	DUMMY	-7890	-313.5
69	VDDB	-7830	-313.5
70	VDDB	-7770	-313.5
71	VDDB	-7710	-313.5
72	VSSB	-7650	-313.5
73	VSSB	-7590	-313.5
74	VSSB	-7530	-313.5
75	VSSB	-7470	-313.5
76	VSSB	-7410	-313.5
77	VSSB	-7350	-313.5
78	VSSB	-7296.	-313.5
79	VSSB	-7230	-313.5
80	VSSB	-7170	-313.5
81	VDDI_OPT	-7110	-313.5
82	LANSEL	-7050	-313.5
83	DSWAP	-6990	-313.5
84	PSWAP	-6930	-313.5
85	VSSI_OPT	-6870	-313.5
86	DUMMY	-6810	-313.5
87	NBWSEL	-6750	-313.5
88	DUMMY	-6690	-313.5
89	DUMMY	-6630	-313.5
90	DUMMY	-6570	-313.5
91	DUMMY	-6510	-313.5
92	VDDI_OPT	-6450	-313.5
93	DUMMY	-6390	-313.5
94	DUMMY	-6330	-313.5
95	IM3	-6270	-313.5
96	IM2	-6210	-313.5
97	IM1	-6150	-313.5
98	IM0	-6090	-313.5
99	DUMMY	-6030	-313.5
100	DUMMY	-5970	-313.5

No.	Pad	X	Y
101	DUMMY	-5910	-313.5
102	OSC_TES	-5850	-313.5
103	OSC_TES	-5790	-313.5
104	DUMMY	-5730	-313.5
105	DUMMY	-5670	-313.5
106	SDO	-5610	-313.5
107	SDI	-5550	-313.5
108	DCX	-5490	-313.5
109	SCL	-5430	-313.5
110	DUMMY	-5370	-313.5
111	CSX	-5310	-313.5
112	RESX	-5250	-313.5
113	VSSB	-5190	-313.5
114	VSSB	-5130	-313.5
115	VSSB	-5070	-313.5
116	VDDI	-5010	-313.5
117	VDDI	-4950	-313.5
118	VDDI	-4890	-313.5
119	D23	-4830	-313.5
120	D22	-4770	-313.5
121	D21	-4710	-313.5
122	D20	-4650	-313.5
123	D19	-4590	-313.5
124	D18	-4530	-313.5
125	D17	-4470	-313.5
126	D16	-4410	-313.5
127	D15	-4350	-313.5
128	D14	-4296.	-313.5
129	D13	-4230	-313.5
130	D12	-4170	-313.5
131	D11	-4110	-313.5
132	D10	-4050	-313.5
133	D9	-3990	-313.5
134	D8	-3930	-313.5
135	D7	-3870	-313.5
136	D6	-3810	-313.5
137	D5	-3750	-313.5
138	D4	-3690	-313.5
139	D3	-3630	-313.5
140	D2	-3570	-313.5
141	D1	-3510	-313.5
142	D0	-3450	-313.5
143	DE	-3390	-313.5
144	PCLK	-3330	-313.5
145	HS	-3270	-313.5
146	VS	-3210	-313.5
147	LEDPWM	-3150	-313.5
148	LEDON	-3090	-313.5
149	DUMMY	-3030	-313.5
150	ERR	-2970	-313.5

No.	Pad	X	Y
151	VDDI	-2910	-313.5
152	VDDI	-2850	-313.5
153	VDDI	-2790	-313.5
154	VSSB	-2730	-313.5
155	VSSB	-2670	-313.5
156	VSSB	-2610	-313.5
157	VDDB	-2550	-313.5
158	VDDB	-2490	-313.5
159	VDDB	-2430	-313.5
160	VDDB	-2370	-313.5
161	VSSB	-2310	-313.5
162	VSSB	-2250	-313.5
163	VSSB	-2190	-313.5
164	VSSB	-2130	-313.5
165	VSSB	-2070	-313.5
166	VSSB	-2010	-313.5
167	VSSB	-1950	-313.5
168	VSSB	-1890	-313.5
169	VSSB	-1830	-313.5
170	VDDB	-1770	-313.5
171	VDDB	-1710	-313.5
172	VDDB	-1650	-313.5
173	VDDB	-1590	-313.5
174	VSSB	-1530	-313.5
175	VSSB	-1470	-313.5
176	VSSB	-1410	-313.5
177	VSSB	-1350	-313.5
178	AVEE	-1296.	-313.5
179	AVEE	-1230	-313.5
180	AVEE	-1170	-313.5
181	AVEE	-1110	-313.5
182	VSSAM	-1050	-313.5
183	VSSAM	-990	-313.5
184	VSSAM	-930	-313.5
185	VSSAM	-870	-313.5
186	VSSAM	-810	-313.5
187	D1_P	-750	-313.5
188	D1_P	-690	-313.5
189	D1_P	-630	-313.5
190	D1_P	-570	-313.5
191	D1_N	-510	-313.5
192	D1_N	-450	-313.5
193	D1_N	-390	-313.5
194	D1_N	-330	-313.5
195	VSSAM	-270	-313.5
196	VSSAM	-210	-313.5
197	CLK_P	-150	-313.5
198	CLK_P	-90	-313.5
199	CLK_P	-30	-313.5
200	CLK_P	30	-313.5

No.	Pad	X	Y
201	CLK_N	90	-313.5
202	CLK_N	150	-313.5
203	CLK_N	210	-313.5
204	CLK_N	270	-313.5
205	VSSAM	330	-313.5
206	VSSAM	390	-313.5
207	D0_P	450	-313.5
208	D0_P	510	-313.5
209	D0_P	570	-313.5
210	D0_P	630	-313.5
211	D0_N	690	-313.5
212	D0_N	750	-313.5
213	D0_N	810	-313.5
214	D0_N	870	-313.5
215	VSSAM	930	-313.5
216	VSSAM	990	-313.5
217	VDDMA	1050	-313.5
218	VDDMA	1110	-313.5
219	VDDMA	1170	-313.5
220	VDDR	1230	-313.5
221	VDDR	1296.	-313.5
222	VDDR	1350	-313.5
223	VDDA	1410	-313.5
224	VDDA	1470	-313.5
225	VDDA	1530	-313.5
226	VDDA	1590	-313.5
227	VDDA	1650	-313.5
228	VDDA	1710	-313.5
229	VDDA	1770	-313.5
230	VDDA	1830	-313.5
231	DMY	1890	-313.5
232	DMY	1950	-313.5
233	VSSR	2010	-313.5
234	VSSR	2070	-313.5
235	VSSR	2130	-313.5
236	VSSR	2190	-313.5
237	VGMP	2250	-313.5
238	VGMP	2310	-313.5
239	DMY	2370	-313.5
240	DMY	2430	-313.5
241	VGSP	2490	-313.5
242	VGSP	2550	-313.5
243	P_GAM	2610	-313.5
244	P_GAM	2670	-313.5
245	VGMN	2730	-313.5
246	VGMN	2790	-313.5
247	N_GAM	2850	-313.5
248	N_GAM	2910	-313.5
249	VDDB	2970	-313.5
250	VDDB	3030	-313.5

No.	Pad	X	Y
251	VDDB	3090	-313.5
252	VDDB	3150	-313.5
253	VDDB	3210	-313.5
254	VDDB	3270	-313.5
255	VSSB	3330	-313.5
256	VSSB	3390	-313.5
257	VSSB	3450	-313.5
258	VSSB	3510	-313.5
259	VSSB	3570	-313.5
260	VSSB	3630	-313.5
261	VREF_T	3690	-313.5
262	VREF_T	3750	-313.5
263	VREF_T	3810	-313.5
264	VDDSF	3870	-313.5
265	VDDSF	3930	-313.5
266	VDDSF	3990	-313.5
267	DVDD	4050	-313.5
268	DVDD	4110	-313.5
269	DVDD	4170	-313.5
270	OTP	4230	-313.5
271	OTP	4296.5	-313.5
272	OTP	4350	-313.5
273	AVDD	4410	-313.5
274	AVDD	4470	-313.5
275	AVDD	4530	-313.5
276	BVEE	4590	-313.5
277	BVEE	4650	-313.5
278	BVEE	4710	-313.5
279	VDDB	4770	-313.5
280	VDDB	4830	-313.5
281	VDDB	4890	-313.5
282	VDDB	4950	-313.5
283	VDDB	5010	-313.5
284	VDDB	5070	-313.5
285	VDDB	5130	-313.5
286	VDDB	5190	-313.5
287	VDDB	5250	-313.5
288	VDDB	5310	-313.5
289	VSSB	5370	-313.5
290	VSSB	5430	-313.5
291	VSSB	5490	-313.5
292	VSSB	5550	-313.5
293	VSSB	5610	-313.5
294	VSSB	5670	-313.5
295	VSSB	5730	-313.5
296	VSSB	5790	-313.5
297	VSSB	5850	-313.5
298	VSSB	5910	-313.5
299	VSSB	5970	-313.5
300	VSSB	6030	-313.5

No.	Pad	X	Y
301	VSSB	6090	-313.5
302	VSSB	6150	-313.5
303	VSSB	6210	-313.5
304	VSSB	6270	-313.5
305	VSSB	6330	-313.5
306	VSSB	6390	-313.5
307	VSSB	6450	-313.5
308	VSSB	6510	-313.5
309	VSSB	6570	-313.5
310	VSSB	6630	-313.5
311	VSSB	6690	-313.5
312	VSSB	6750	-313.5
313	VSSB	6810	-313.5
314	VSSB	6870	-313.5
315	VDDB	6930	-313.5
316	VDDB	6990	-313.5
317	VDDB	7050	-313.5
318	VDDB	7110	-313.5
319	VDDB	7170	-313.5
320	VDDB	7230	-313.5
321	VDDB	7296.5	-313.5
322	VDDB	7350	-313.5
323	VDDB	7410	-313.5
324	VDDB	7470	-313.5
325	VDDB	7530	-313.5
326	VDDB	7590	-313.5
327	VDDB	7650	-313.5
328	VDDB	7710	-313.5
329	VSSB	7770	-313.5
330	VSSB	7830	-313.5
331	VSSB	7890	-313.5
332	VSSB	7950	-313.5
333	VSSB	8010	-313.5
334	VSSB	8070	-313.5
335	VSSB	8130	-313.5
336	VSSB	8190	-313.5
337	VSSB	8250	-313.5
338	VSSB	8310	-313.5
339	DVSS	8370	-313.5
340	DVSS	8430	-313.5
341	DVSS	8490	-313.5
342	DVSS	8550	-313.5
343	VDDB	8610	-313.5
344	VDDB	8670	-313.5
345	VDDB	8730	-313.5
346	VDDB	8790	-313.5
347	VDDB	8850	-313.5
348	VDDB	8910	-313.5
349	VDDB	8970	-313.5
350	VDDB	9030	-313.5

No.	Pad	X	Y
351	VDDB	9090	-313.5
352	VDH	9150	-313.5
353	VDH	9210	-313.5
354	VDH	9270	-313.5
355	DUMMY	9330	-313.5
356	DUMMY	9390	-313.5
357	DUMMY	9450	-313.5
358	VSSB	9510	-313.5
359	VSSB	9570	-313.5
360	VSSB	9630	-313.5
361	VSSB	9690	-313.5
362	VSSB	9750	-313.5
363	VSSB	9810	-313.5
364	VSSB	9870	-313.5
365	VGH	9930	-313.5
366	VGH	9990	-313.5
367	VGH	10050	-313.5
368	VGH	10110	-313.5
369	DUMMY	10170	-313.5
370	DUMMY	10230	-313.5
371	VDDB	10296	-313.5
372	VDDB	10350	-313.5
373	VDDB	10410	-313.5
374	VDDB	10470	-313.5
375	DUMMY	10530	-313.5
376	DUMMY	10590	-313.5
377	VGL	10650	-313.5
378	VGL	10710	-313.5
379	VGL	10770	-313.5
380	VGL	10830	-313.5
381	VGL	10890	-313.5
382	VGL	10950	-313.5
383	DUMMY	11010	-313.5
384	DUMMY	11070	-313.5
385	DUMMY	11130	-313.5
386	DUMMY	11190	-313.5
387	DUMMY	11250	-313.5
388	DUMMY	11310	-313.5
389	VCOM	11370	-313.5
390	VCOM	11430	-313.5
391	VCOM	11490	-313.5
392	VCOM	11550	-313.5
393	VCOM	11610	-313.5
394	DMY	11670	-313.5
395	DMY	11730	-313.5
396	DMY	11790	-313.5
397	DMY	11850	-313.5
398	DMY	11910	-313.5
399	DUMMY	11760	296.5
400	DUMMY	11732	168.5

No.	Pad	X	Y
401	DUMMY	11718	296.5
402	DUMMY	11704	168.5
403	DUMMY	11690	296.5
404	VGHO	11676	168.5
405	VGHO	11662	296.5
406	VGHO	11648	168.5
407	GOUT_VGL	11634	296.5
408	GOUT_VGL	11620	168.5
409	GOUT_VGL	11606	296.5
410	GOUT1	11592	168.5
411	GOUT1	11578	296.5
412	GOUT2	11564	168.5
413	GOUT2	11550	296.5
414	LVGL	11536	168.5
415	LVGL	11522	296.5
416	VGLO	11508	168.5
417	VRGH	11494	296.5
418	VRGH	11480	168.5
419	VRGH	11466	296.5
420	GOUT_VGL	11452	168.5
421	GOUT_VGL	11438	296.5
422	GOUT_VGL	11424	168.5
423	GOUT3	11410	296.5
424	GOUT3	11396	168.5
425	GOUT4	11382	296.5
426	GOUT4	11368	168.5
427	GOUT5	11354	296.5
428	GOUT5	11340	168.5
429	GOUT6	11326	296.5
430	GOUT6	11312	168.5
431	GOUT7	11298	296.5
432	GOUT7	11284	168.5
433	GOUT8	11270	296.5
434	GOUT8	11256	168.5
435	GOUT9	11242	296.5
436	GOUT9	11228	168.5
437	GOUT10	11214	296.5
438	GOUT10	11200	168.5
439	GOUT11	11186	296.5
440	GOUT11	11172	168.5
441	GOUT12	11158	296.5
442	GOUT12	11144	168.5
443	GOUT13	11130	296.5
444	GOUT13	11116	168.5
445	GOUT14	11102	296.5
446	GOUT14	11088	168.5
447	GOUT15	11074	296.5
448	GOUT15	11060	168.5
449	GOUT16	11046	296.5
450	GOUT16	11032	168.5

No.	Pad	X	Y
451	VGH	11018	296.5
452	VGH	11004	168.5
453	VGH	10990	296.5
454	VGH	10976	168.5
455	VGH	10962	296.5
456	VGH	10948	168.5
457	VGH	10934	296.5
458	VGH	10920	168.5
459	VGLO	10906	296.5
460	VGLO	10892	168.5
461	VGLO	10878	296.5
462	VGLO	10864	168.5
463	VGLO	10850	296.5
464	VGLO	10836	168.5
465	SDU	10738	296.5
466	S1	10724	168.5
467	S2	10710	296.5
468	S3	10696	168.5
469	S4	10682	296.5
470	S5	10668	168.5
471	S6	10654	296.5
472	S7	10640	168.5
473	S8	10626	296.5
474	S9	10612	168.5
475	S10	10598	296.5
476	S11	10584	168.5
477	S12	10570	296.5
478	S13	10556	168.5
479	S14	10542	296.5
480	S15	10528	168.5
481	S16	10514	296.5
482	S17	10500	168.5
483	S18	10486	296.5
484	S19	10472	168.5
485	S20	10458	296.5
486	S21	10444	168.5
487	S22	10430	296.5
488	S23	10416	168.5
489	S24	10402	296.5
490	S25	10388	168.5
491	S26	10374	296.5
492	S27	10360	168.5
493	S28	10346	296.5
494	S29	10332	168.5
495	S30	10318	296.5
496	S31	10304	168.5
497	S32	10296.5	296.5
498	S33	10276	168.5
499	S34	10262	296.5
500	S35	10248	168.5

No.	Pad	X	Y
501	S36	10234	296.5
502	S37	10220	168.5
503	S38	10206	296.5
504	S39	10192	168.5
505	S40	10178	296.5
506	S41	10164	168.5
507	S42	10150	296.5
508	S43	10136	168.5
509	S44	10122	296.5
510	S45	10108	168.5
511	S46	10094	296.5
512	S47	10080	168.5
513	S48	10066	296.5
514	S49	10052	168.5
515	S50	10038	296.5
516	S51	10024	168.5
517	S52	10010	296.5
518	S53	9996	168.5
519	S54	9982	296.5
520	S55	9968	168.5
521	S56	9954	296.5
522	S57	9940	168.5
523	S58	9926	296.5
524	S59	9912	168.5
525	S60	9898	296.5
526	S61	9884	168.5
527	S62	9870	296.5
528	S63	9856	168.5
529	S64	9842	296.5
530	S65	9828	168.5
531	S66	9814	296.5
532	S67	9800	168.5
533	S68	9786	296.5
534	S69	9772	168.5
535	S70	9758	296.5
536	S71	9744	168.5
537	S72	9730	296.5
538	S73	9716	168.5
539	S74	9702	296.5
540	S75	9688	168.5
541	S76	9674	296.5
542	S77	9660	168.5
543	S78	9646	296.5
544	S79	9632	168.5
545	S80	9618	296.5
546	S81	9604	168.5
547	S82	9590	296.5
548	S83	9576	168.5
549	S84	9562	296.5
550	S85	9548	168.5

No.	Pad	X	Y
551	S86	9534	296.5
552	S87	9520	168.5
553	S88	9506	296.5
554	S89	9492	168.5
555	S90	9478	296.5
556	S91	9464	168.5
557	S92	9450	296.5
558	S93	9436	168.5
559	S94	9422	296.5
560	S95	9408	168.5
561	S96	9394	296.5
562	S97	9380	168.5
563	S98	9366	296.5
564	S99	9352	168.5
565	S100	9338	296.5
566	S101	9324	168.5
567	S102	9310	296.5
568	S103	9296	168.5
569	S104	9282	296.5
570	S105	9268	168.5
571	S106	9254	296.5
572	S107	9240	168.5
573	S108	9226	296.5
574	S109	9212	168.5
575	S110	9198	296.5
576	S111	9184	168.5
577	S112	9170	296.5
578	S113	9156	168.5
579	S114	9142	296.5
580	S115	9128	168.5
581	S116	9114	296.5
582	S117	9100	168.5
583	S118	9086	296.5
584	S119	9072	168.5
585	S120	9058	296.5
586	S121	9044	168.5
587	S122	9030	296.5
588	S123	9016	168.5
589	S124	9002	296.5
590	S125	8988	168.5
591	S126	8974	296.5
592	S127	8960	168.5
593	S128	8946	296.5
594	S129	8932	168.5
595	S130	8918	296.5
596	S131	8904	168.5
597	S132	8890	296.5
598	S133	8876	168.5
599	S134	8862	296.5
600	S135	8848	168.5

No.	Pad	X	Y
601	S136	8834	296.5
602	S137	8820	168.5
603	S138	8806	296.5
604	S139	8792	168.5
605	S140	8778	296.5
606	S141	8764	168.5
607	S142	8750	296.5
608	S143	8736	168.5
609	S144	8722	296.5
610	S145	8708	168.5
611	S146	8694	296.5
612	S147	8680	168.5
613	S148	8666	296.5
614	S149	8652	168.5
615	S150	8638	296.5
616	S151	8624	168.5
617	S152	8610	296.5
618	S153	8596	168.5
619	S154	8582	296.5
620	S155	8568	168.5
621	S156	8554	296.5
622	S157	8540	168.5
623	S158	8526	296.5
624	S159	8512	168.5
625	S160	8498	296.5
626	S161	8484	168.5
627	S162	8470	296.5
628	S163	8456	168.5
629	S164	8442	296.5
630	S165	8428	168.5
631	S166	8414	296.5
632	S167	8400	168.5
633	S168	8386	296.5
634	S169	8372	168.5
635	S170	8358	296.5
636	S171	8344	168.5
637	S172	8330	296.5
638	S173	8316	168.5
639	S174	8302	296.5
640	S175	8288	168.5
641	S176	8274	296.5
642	S177	8260	168.5
643	S178	8246	296.5
644	S179	8232	168.5
645	S180	8218	296.5
646	S181	8204	168.5
647	S182	8190	296.5
648	S183	8176	168.5
649	S184	8162	296.5
650	S185	8148	168.5
651	S186	8134	296.5
652	S187	8120	168.5
653	S188	8106	296.5
654	S189	8092	168.5
655	S190	8078	296.5
656	S191	8064	168.5
657	S192	8050	296.5
658	S193	8036	168.5
659	S194	8022	296.5
660	S195	8008	168.5
661	S196	7994	296.5
662	S197	7980	168.5
663	S198	7966	296.5
664	S199	7952	168.5
665	S200	7938	296.5
666	S201	7924	168.5
667	S202	7910	296.5
668	S203	7896	168.5
669	S204	7882	296.5
670	S205	7868	168.5
671	S206	7854	296.5
672	S207	7840	168.5
673	S208	7826	296.5
674	S209	7812	168.5
675	S210	7798	296.5
676	S211	7784	168.5
677	S212	7770	296.5
678	S213	7756	168.5
679	S214	7742	296.5
680	S215	7728	168.5
681	S216	7714	296.5
682	S217	7700	168.5
683	S218	7686	296.5
684	S219	7672	168.5
685	S220	7658	296.5
686	S221	7644	168.5
687	S222	7630	296.5
688	S223	7616	168.5
689	S224	7602	296.5
690	S225	7588	168.5
691	S226	7574	296.5
692	S227	7560	168.5
693	S228	7546	296.5
694	S229	7532	168.5
695	S230	7518	296.5
696	S231	7504	168.5
697	S232	7490	296.5
698	S233	7476	168.5
699	S234	7462	296.5
700	S235	7448	168.5
701	S236	7434	296.5
702	S237	7420	168.5
703	S238	7406	296.5
704	S239	7392	168.5
705	S240	7378	296.5
706	S241	7364	168.5
707	S242	7350	296.5
708	S243	7336	168.5
709	S244	7322	296.5
710	S245	7308	168.5
711	S246	7294	296.5
712	S247	7280	168.5
713	S248	7266	296.5
714	S249	7252	168.5
715	S250	7238	296.5
716	S251	7224	168.5
717	S252	7210	296.5
718	S253	7196	168.5
719	S254	7182	296.5
720	S255	7168	168.5
721	S256	7154	296.5
722	S257	7140	168.5
723	S258	7126	296.5
724	S259	7112	168.5
725	S260	7098	296.5
726	S261	7084	168.5
727	S262	7070	296.5
728	S263	7056	168.5
729	S264	7042	296.5
730	S265	7028	168.5
731	S266	7014	296.5
732	S267	7000	168.5
733	S268	6986	296.5
734	S269	6972	168.5
735	S270	6958	296.5
736	S271	6944	168.5
737	S272	6930	296.5
738	S273	6916	168.5
739	S274	6902	296.5
740	S275	6888	168.5
741	S276	6874	296.5
742	S277	6860	168.5
743	S278	6846	296.5
744	S279	6832	168.5
745	S280	6818	296.5
746	S281	6804	168.5
747	S282	6790	296.5
748	S283	6776	168.5
749	S284	6762	296.5
750	S285	6748	168.5

No.	Pad	X	Y
751	S286	6734	296.5
752	S287	6720	168.5
753	S288	6706	296.5
754	S289	6692	168.5
755	S290	6678	296.5
756	S291	6664	168.5
757	S292	6650	296.5
758	S293	6636	168.5
759	S294	6622	296.5
760	S295	6608	168.5
761	S296	6594	296.5
762	S297	6580	168.5
763	S298	6566	296.5
764	S299	6552	168.5
765	S300	6538	296.5
766	S301	6524	168.5
767	S302	6510	296.5
768	S303	6496	168.5
769	S304	6482	296.5
770	S305	6468	168.5
771	S306	6454	296.5
772	S307	6440	168.5
773	S308	6426	296.5
774	S309	6412	168.5
775	S310	6398	296.5
776	S311	6384	168.5
777	S312	6370	296.5
778	S313	6356	168.5
779	S314	6342	296.5
780	S315	6328	168.5
781	S316	6314	296.5
782	S317	6300	168.5
783	S318	6286	296.5
784	S319	6272	168.5
785	S320	6258	296.5
786	S321	6244	168.5
787	S322	6230	296.5
788	S323	6216	168.5
789	S324	6202	296.5
790	S325	6188	168.5
791	S326	6174	296.5
792	S327	6160	168.5
793	S328	6146	296.5
794	S329	6132	168.5
795	S330	6118	296.5
796	S331	6104	168.5
797	S332	6090	296.5
798	S333	6076	168.5
799	S334	6062	296.5
800	S335	6048	168.5

No.	Pad	X	Y
801	S336	6034	296.5
802	S337	6020	168.5
803	S338	6006	296.5
804	S339	5992	168.5
805	S340	5978	296.5
806	S341	5964	168.5
807	S342	5950	296.5
808	S343	5936	168.5
809	S344	5922	296.5
810	S345	5908	168.5
811	S346	5894	296.5
812	S347	5880	168.5
813	S348	5866	296.5
814	S349	5852	168.5
815	S350	5838	296.5
816	S351	5824	168.5
817	S352	5810	296.5
818	S353	5796	168.5
819	S354	5782	296.5
820	S355	5768	168.5
821	S356	5754	296.5
822	S357	5740	168.5
823	S358	5726	296.5
824	S359	5712	168.5
825	S360	5698	296.5
826	S361	5684	168.5
827	S362	5670	296.5
828	S363	5656	168.5
829	S364	5642	296.5
830	S365	5628	168.5
831	S366	5614	296.5
832	S367	5600	168.5
833	S368	5586	296.5
834	S369	5572	168.5
835	S370	5558	296.5
836	S371	5544	168.5
837	S372	5530	296.5
838	S373	5516	168.5
839	S374	5502	296.5
840	S375	5488	168.5
841	S376	5474	296.5
842	S377	5460	168.5
843	S378	5446	296.5
844	S379	5432	168.5
845	S380	5418	296.5
846	S381	5404	168.5
847	S382	5390	296.5
848	S383	5376	168.5
849	S384	5362	296.5
850	S385	5348	168.5

No.	Pad	X	Y
851	S386	5334	296.5
852	S387	5320	168.5
853	S388	5306	296.5
854	S389	5292	168.5
855	S390	5278	296.5
856	S391	5264	168.5
857	S392	5250	296.5
858	S393	5236	168.5
859	S394	5222	296.5
860	S395	5208	168.5
861	S396	5194	296.5
862	S397	5180	168.5
863	S398	5166	296.5
864	S399	5152	168.5
865	S400	5138	296.5
866	S401	5124	168.5
867	S402	5110	296.5
868	S403	5096	168.5
869	S404	5082	296.5
870	S405	5068	168.5
871	S406	5054	296.5
872	S407	5040	168.5
873	S408	5026	296.5
874	S409	5012	168.5
875	S410	4998	296.5
876	S411	4984	168.5
877	S412	4970	296.5
878	S413	4956	168.5
879	S414	4942	296.5
880	S415	4928	168.5
881	S416	4914	296.5
882	S417	4900	168.5
883	S418	4886	296.5
884	S419	4872	168.5
885	S420	4858	296.5
886	S421	4844	168.5
887	S422	4830	296.5
888	S423	4816	168.5
889	S424	4802	296.5
890	S425	4788	168.5
891	S426	4774	296.5
892	S427	4760	168.5
893	S428	4746	296.5
894	S429	4732	168.5
895	S430	4718	296.5
896	S431	4704	168.5
897	S432	4690	296.5
898	S433	4676	168.5
899	S434	4662	296.5
900	S435	4648	168.5

No.	Pad	X	Y
901	S436	4634	296.5
902	S437	4620	168.5
903	S438	4606	296.5
904	S439	4592	168.5
905	S440	4578	296.5
906	S441	4564	168.5
907	S442	4550	296.5
908	S443	4536	168.5
909	S444	4522	296.5
910	S445	4508	168.5
911	S446	4494	296.5
912	S447	4480	168.5
913	S448	4466	296.5
914	S449	4452	168.5
915	S450	4438	296.5
916	S451	4424	168.5
917	S452	4410	296.5
918	S453	4396	168.5
919	S454	4382	296.5
920	S455	4368	168.5
921	S456	4354	296.5
922	S457	4340	168.5
923	S458	4326	296.5
924	S459	4312	168.5
925	S460	4298	296.5
926	S461	4284	168.5
927	S462	4270	296.5
928	S463	4256	168.5
929	S464	4242	296.5
930	S465	4228	168.5
931	S466	4214	296.5
932	S467	4200	168.5
933	S468	4186	296.5
934	S469	4172	168.5
935	S470	4158	296.5
936	S471	4144	168.5
937	S472	4130	296.5
938	S473	4116	168.5
939	S474	4102	296.5
940	S475	4088	168.5
941	S476	4074	296.5
942	S477	4060	168.5
943	S478	4046	296.5
944	S479	4032	168.5
945	S480	4018	296.5
946	S481	4004	168.5
947	S482	3990	296.5
948	S483	3976	168.5
949	S484	3962	296.5
950	S485	3948	168.5

No.	Pad	X	Y
951	S486	3934	296.5
952	S487	3920	168.5
953	S488	3906	296.5
954	S489	3892	168.5
955	S490	3878	296.5
956	S491	3864	168.5
957	S492	3850	296.5
958	S493	3836	168.5
959	S494	3822	296.5
960	S495	3808	168.5
961	S496	3794	296.5
962	S497	3780	168.5
963	S498	3766	296.5
964	S499	3752	168.5
965	S500	3738	296.5
966	S501	3724	168.5
967	S502	3710	296.5
968	S503	3696	168.5
969	S504	3682	296.5
970	S505	3668	168.5
971	S506	3654	296.5
972	S507	3640	168.5
973	S508	3626	296.5
974	S509	3612	168.5
975	S510	3598	296.5
976	S511	3584	168.5
977	S512	3570	296.5
978	S513	3556	168.5
979	S514	3542	296.5
980	S515	3528	168.5
981	S516	3514	296.5
982	S517	3500	168.5
983	S518	3486	296.5
984	S519	3472	168.5
985	S520	3458	296.5
986	S521	3444	168.5
987	S522	3430	296.5
988	S523	3416	168.5
989	S524	3402	296.5
990	S525	3388	168.5
991	S526	3374	296.5
992	S527	3360	168.5
993	S528	3346	296.5
994	S529	3332	168.5
995	S530	3318	296.5
996	S531	3304	168.5
997	S532	3296.	296.5
998	S533	3276	168.5
999	S534	3262	296.5
1000	S535	3248	168.5

No.	Pad	X	Y
1001	S536	3234	296.5
1002	S537	3220	168.5
1003	S538	3206	296.5
1004	S539	3192	168.5
1005	S540	3178	296.5
1006	S541	3164	168.5
1007	S542	3150	296.5
1008	S543	3136	168.5
1009	S544	3122	296.5
1010	S545	3108	168.5
1011	S546	3094	296.5
1012	S547	3080	168.5
1013	S548	3066	296.5
1014	S549	3052	168.5
1015	S550	3038	296.5
1016	S551	3024	168.5
1017	S552	3010	296.5
1018	S553	2996	168.5
1019	S554	2982	296.5
1020	S555	2968	168.5
1021	S556	2954	296.5
1022	S557	2940	168.5
1023	S558	2926	296.5
1024	S559	2912	168.5
1025	S560	2898	296.5
1026	S561	2884	168.5
1027	S562	2870	296.5
1028	S563	2856	168.5
1029	S564	2842	296.5
1030	S565	2828	168.5
1031	S566	2814	296.5
1032	S567	2800	168.5
1033	S568	2786	296.5
1034	S569	2772	168.5
1035	S570	2758	296.5
1036	S571	2744	168.5
1037	S572	2730	296.5
1038	S573	2716	168.5
1039	S574	2702	296.5
1040	S575	2688	168.5
1041	S576	2674	296.5
1042	S577	2660	168.5
1043	S578	2646	296.5
1044	S579	2632	168.5
1045	S580	2618	296.5
1046	S581	2604	168.5
1047	S582	2590	296.5
1048	S583	2576	168.5
1049	S584	2562	296.5
1050	S585	2548	168.5

No.	Pad	X	Y
1051	S586	2534	296.5
1052	S587	2520	168.5
1053	S588	2506	296.5
1054	S589	2492	168.5
1055	S590	2478	296.5
1056	S591	2464	168.5
1057	S592	2450	296.5
1058	S593	2436	168.5
1059	S594	2422	296.5
1060	S595	2408	168.5
1061	S596	2394	296.5
1062	S597	2380	168.5
1063	S598	2366	296.5
1064	S599	2352	168.5
1065	S600	2338	296.5
1066	S601	2324	168.5
1067	S602	2310	296.5
1068	S603	2296	168.5
1069	S604	2282	296.5
1070	S605	2268	168.5
1071	S606	2254	296.5
1072	S607	2240	168.5
1073	S608	2226	296.5
1074	S609	2212	168.5
1075	S610	2198	296.5
1076	S611	2184	168.5
1077	S612	2170	296.5
1078	S613	2156	168.5
1079	S614	2142	296.5
1080	S615	2128	168.5
1081	S616	2114	296.5
1082	S617	2100	168.5
1083	S618	2086	296.5
1084	S619	2072	168.5
1085	S620	2058	296.5
1086	S621	2044	168.5
1087	S622	2030	296.5
1088	S623	2016	168.5
1089	S624	2002	296.5
1090	S625	1988	168.5
1091	S626	1974	296.5
1092	S627	1960	168.5
1093	S628	1946	296.5
1094	S629	1932	168.5
1095	S630	1918	296.5
1096	S631	1904	168.5
1097	S632	1890	296.5
1098	S633	1876	168.5
1099	S634	1862	296.5
1100	S635	1848	168.5

No.	Pad	X	Y
1101	S636	1834	296.5
1102	S637	1820	168.5
1103	S638	1806	296.5
1104	S639	1792	168.5
1105	S640	1778	296.5
1106	S641	1764	168.5
1107	S642	168.5	296.5
1108	S643	1736	168.5
1109	S644	1722	296.5
1110	S645	1708	168.5
1111	S646	1694	296.5
1112	S647	1680	168.5
1113	S648	1666	296.5
1114	S649	1652	168.5
1115	S650	1638	296.5
1116	S651	1624	168.5
1117	S652	1610	296.5
1118	S653	1596	168.5
1119	S654	1582	296.5
1120	S655	1568	168.5
1121	S656	1554	296.5
1122	S657	1540	168.5
1123	S658	1526	296.5
1124	S659	1512	168.5
1125	S660	1498	296.5
1126	S661	1484	168.5
1127	S662	1470	296.5
1128	S663	1456	168.5
1129	S664	1442	296.5
1130	S665	1428	168.5
1131	S666	1414	296.5
1132	S667	1400	168.5
1133	S668	1386	296.5
1134	S669	1372	168.5
1135	S670	1358	296.5
1136	S671	1344	168.5
1137	S672	1330	296.5
1138	S673	1316	168.5
1139	S674	1302	296.5
1140	S675	1288	168.5
1141	S676	1274	296.5
1142	S677	1260	168.5
1143	S678	1246	296.5
1144	S679	1232	168.5
1145	S680	1218	296.5
1146	S681	1204	168.5
1147	S682	1190	296.5
1148	S683	1176	168.5
1149	S684	1162	296.5
1150	S685	1148	168.5

No.	Pad	X	Y
1151	S686	1134	296.5
1152	S687	1120	168.5
1153	S688	1106	296.5
1154	S689	1092	168.5
1155	S690	1078	296.5
1156	S691	1064	168.5
1157	S692	1050	296.5
1158	S693	1036	168.5
1159	S694	1022	296.5
1160	S695	1008	168.5
1161	S696	994	296.5
1162	S697	980	168.5
1163	S698	966	296.5
1164	S699	952	168.5
1165	S700	938	296.5
1166	S701	924	168.5
1167	S702	910	296.5
1168	S703	896	168.5
1169	S704	882	296.5
1170	S705	868	168.5
1171	S706	854	296.5
1172	S707	840	168.5
1173	S708	826	296.5
1174	S709	812	168.5
1175	S710	798	296.5
1176	S711	784	168.5
1177	S712	770	296.5
1178	S713	756	168.5
1179	S714	742	296.5
1180	S715	728	168.5
1181	S716	714	296.5
1182	S717	700	168.5
1183	S718	686	296.5
1184	S719	672	168.5
1185	S720	658	296.5
1186	VSSIDUM9	644	168.5
1187	VSSIDUM1	630	296.5
1188	VSSIDUM1	616	168.5
1189	VSSIDUM1	602	296.5
1190	VSSIDUM1	588	168.5
1191	VSSIDUM1	574	296.5
1192	VSSIDUM1	560	168.5
1193	VSSIDUM1	546	296.5
1194	VSSIDUM1	532	168.5
1195	VSSIDUM1	518	296.5
1196	VSSIDUM1	504	168.5
1197	VSSIDUM2	490	296.5
1198	VSSIDUM2	476	168.5
1199	VSSIDUM2	462	296.5
1200	VSSIDUM2	448	168.5

No.	Pad	X	Y
1201	VSSI	434	296.5
1202	VSSI	420	168.5
1203	VSSI	406	296.5
1204	VSSI	392	168.5
1205	VSSI	378	296.5
1206	VSSI	364	168.5
1207	VSSI	350	296.5
1208	VSSI	336	168.5
1209	VSSI	322	296.5
1210	VSSI	308	168.5
1211	VSSI	294	296.5
1212	VSSI	280	168.5
1213	VSSI	266	296.5
1214	VSSI	252	168.5
1215	VSSI	238	296.5
1216	VSSI	224	168.5
1217	VSSI	210	296.5
1218	VSSI	196	168.5
1219	VSSI	182	296.5
1220	VSSI	168	168.5
1221	VSSI	154	296.5
1222	VSSI	140	168.5
1223	VSSI	126	296.5
1224	VSSI	112	168.5
1225	VSSI	98	296.5
1226	VSSI	84	168.5
1227	VSSI	70	296.5
1228	VSSI	56	168.5
1229	VSSI	42	296.5
1230	VSSI	28	168.5
1231	VSSI	14	296.5
1232	VSSI	0	168.5
1233	VSSI	-14	296.5
1234	VSSI	-28	168.5
1235	S721	-42	296.5
1236	S722	-56	168.5
1237	S723	-70	296.5
1238	S724	-84	168.5
1239	S725	-98	296.5
1240	S726	-112	168.5
1241	S727	-126	296.5
1242	S728	-140	168.5
1243	S729	-154	296.5
1244	S730	-168	168.5
1245	S731	-182	296.5
1246	S732	-196	168.5
1247	S733	-210	296.5
1248	S734	-224	168.5
1249	S735	-238	296.5
1250	S736	-252	168.5
1251	S737	-266	296.5
1252	S738	-280	168.5
1253	S739	-294	296.5
1254	S740	-308	168.5
1255	S741	-322	296.5
1256	S742	-336	168.5
1257	S743	-350	296.5
1258	S744	-364	168.5
1259	S745	-378	296.5
1260	S746	-392	168.5
1261	S747	-406	296.5
1262	S748	-420	168.5
1263	S749	-434	296.5
1264	S750	-448	168.5
1265	S751	-462	296.5
1266	S752	-476	168.5
1267	S753	-490	296.5
1268	S754	-504	168.5
1269	S755	-518	296.5
1270	S756	-532	168.5
1271	S757	-546	296.5
1272	S758	-560	168.5
1273	S759	-574	296.5
1274	S760	-588	168.5
1275	S761	-602	296.5
1276	S762	-616	168.5
1277	S763	-630	296.5
1278	S764	-644	168.5
1279	S765	-658	296.5
1280	S766	-672	168.5
1281	S767	-686	296.5
1282	S768	-700	168.5
1283	S769	-714	296.5
1284	S770	-728	168.5
1285	S771	-742	296.5
1286	S772	-756	168.5
1287	S773	-770	296.5
1288	S774	-784	168.5
1289	S775	-798	296.5
1290	S776	-812	168.5
1291	S777	-826	296.5
1292	S778	-840	168.5
1293	S779	-854	296.5
1294	S780	-868	168.5
1295	S781	-882	296.5
1296	S782	-896	168.5
1297	S783	-910	296.5
1298	S784	-924	168.5
1299	S785	-938	296.5
1300	S786	-952	168.5
1301	S787	-966	296.5
1302	S788	-980	168.5
1303	S789	-994	296.5
1304	S790	-1008	168.5
1305	S791	-1022	296.5
1306	S792	-1036	168.5
1307	S793	-1050	296.5
1308	S794	-1064	168.5
1309	S795	-1078	296.5
1310	S796	-1092	168.5
1311	S797	-1106	296.5
1312	S798	-1120	168.5
1313	S799	-1134	296.5
1314	S800	-1148	168.5
1315	S801	-1162	296.5
1316	S802	-1176	168.5
1317	S803	-1190	296.5
1318	S804	-1204	168.5
1319	S805	-1218	296.5
1320	S806	-1232	168.5
1321	S807	-1246	296.5
1322	S808	-1260	168.5
1323	S809	-1274	296.5
1324	S810	-1288	168.5
1325	S811	-1302	296.5
1326	S812	-1316	168.5
1327	S813	-1330	296.5
1328	S814	-1344	168.5
1329	S815	-1358	296.5
1330	S816	-1372	168.5
1331	S817	-1386	296.5
1332	S818	-1400	168.5
1333	S819	-1414	296.5
1334	S820	-1428	168.5
1335	S821	-1442	296.5
1336	S822	-1456	168.5
1337	S823	-1470	296.5
1338	S824	-1484	168.5
1339	S825	-1498	296.5
1340	S826	-1512	168.5
1341	S827	-1526	296.5
1342	S828	-1540	168.5
1343	S829	-1554	296.5
1344	S830	-1568	168.5
1345	S831	-1582	296.5
1346	S832	-1596	168.5
1347	S833	-1610	296.5
1348	S834	-1624	168.5
1349	S835	-1638	296.5
1350	S836	-1652	168.5

No.	Pad	X	Y
1351	S837	-1666	296.5
1352	S838	-1680	168.5
1353	S839	-1694	296.5
1354	S840	-1708	168.5
1355	S841	-1722	296.5
1356	S842	-1736	168.5
1357	S843	-168.5	296.5
1358	S844	-1764	168.5
1359	S845	-1778	296.5
1360	S846	-1792	168.5
1361	S847	-1806	296.5
1362	S848	-1820	168.5
1363	S849	-1834	296.5
1364	S850	-1848	168.5
1365	S851	-1862	296.5
1366	S852	-1876	168.5
1367	S853	-1890	296.5
1368	S854	-1904	168.5
1369	S855	-1918	296.5
1370	S856	-1932	168.5
1371	S857	-1946	296.5
1372	S858	-1960	168.5
1373	S859	-1974	296.5
1374	S860	-1988	168.5
1375	S861	-2002	296.5
1376	S862	-2016	168.5
1377	S863	-2030	296.5
1378	S864	-2044	168.5
1379	S865	-2058	296.5
1380	S866	-2072	168.5
1381	S867	-2086	296.5
1382	S868	-2100	168.5
1383	S869	-2114	296.5
1384	S870	-2128	168.5
1385	S871	-2142	296.5
1386	S872	-2156	168.5
1387	S873	-2170	296.5
1388	S874	-2184	168.5
1389	S875	-2198	296.5
1390	S876	-2212	168.5
1391	S877	-2226	296.5
1392	S878	-2240	168.5
1393	S879	-2254	296.5
1394	S880	-2268	168.5
1395	S881	-2282	296.5
1396	S882	-2296	168.5
1397	S883	-2310	296.5
1398	S884	-2324	168.5
1399	S885	-2338	296.5
1400	S886	-2352	168.5

No.	Pad	X	Y
1401	S887	-2366	296.5
1402	S888	-2380	168.5
1403	S889	-2394	296.5
1404	S890	-2408	168.5
1405	S891	-2422	296.5
1406	S892	-2436	168.5
1407	S893	-2450	296.5
1408	S894	-2464	168.5
1409	S895	-2478	296.5
1410	S896	-2492	168.5
1411	S897	-2506	296.5
1412	S898	-2520	168.5
1413	S899	-2534	296.5
1414	S900	-2548	168.5
1415	S901	-2562	296.5
1416	S902	-2576	168.5
1417	S903	-2590	296.5
1418	S904	-2604	168.5
1419	S905	-2618	296.5
1420	S906	-2632	168.5
1421	S907	-2646	296.5
1422	S908	-2660	168.5
1423	S909	-2674	296.5
1424	S910	-2688	168.5
1425	S911	-2702	296.5
1426	S912	-2716	168.5
1427	S913	-2730	296.5
1428	S914	-2744	168.5
1429	S915	-2758	296.5
1430	S916	-2772	168.5
1431	S917	-2786	296.5
1432	S918	-2800	168.5
1433	S919	-2814	296.5
1434	S920	-2828	168.5
1435	S921	-2842	296.5
1436	S922	-2856	168.5
1437	S923	-2870	296.5
1438	S924	-2884	168.5
1439	S925	-2898	296.5
1440	S926	-2912	168.5
1441	S927	-2926	296.5
1442	S928	-2940	168.5
1443	S929	-2954	296.5
1444	S930	-2968	168.5
1445	S931	-2982	296.5
1446	S932	-2996	168.5
1447	S933	-3010	296.5
1448	S934	-3024	168.5
1449	S935	-3038	296.5
1450	S936	-3052	168.5

No.	Pad	X	Y
1451	S937	-313.5	296.5
1452	S938	-3080	168.5
1453	S939	-3094	296.5
1454	S940	-3108	168.5
1455	S941	-3122	296.5
1456	S942	-3136	168.5
1457	S943	-3150	296.5
1458	S944	-3164	168.5
1459	S945	-3178	296.5
1460	S946	-3192	168.5
1461	S947	-3206	296.5
1462	S948	-3220	168.5
1463	S949	-3234	296.5
1464	S950	-3248	168.5
1465	S951	-3262	296.5
1466	S952	-3276	168.5
1467	S953	-3296.	296.5
1468	S954	-3304	168.5
1469	S955	-3318	296.5
1470	S956	-3332	168.5
1471	S957	-3346	296.5
1472	S958	-3360	168.5
1473	S959	-3374	296.5
1474	S960	-3388	168.5
1475	S961	-3402	296.5
1476	S962	-3416	168.5
1477	S963	-3430	296.5
1478	S964	-3444	168.5
1479	S965	-3458	296.5
1480	S966	-3472	168.5
1481	S967	-3486	296.5
1482	S968	-3500	168.5
1483	S969	-3514	296.5
1484	S970	-3528	168.5
1485	S971	-3542	296.5
1486	S972	-3556	168.5
1487	S973	-3570	296.5
1488	S974	-3584	168.5
1489	S975	-3598	296.5
1490	S976	-3612	168.5
1491	S977	-3626	296.5
1492	S978	-3640	168.5
1493	S979	-3654	296.5
1494	S980	-3668	168.5
1495	S981	-3682	296.5
1496	S982	-3696	168.5
1497	S983	-3710	296.5
1498	S984	-3724	168.5
1499	S985	-3738	296.5
1500	S986	-3752	168.5

No.	Pad	X	Y
1501	S987	-3766	296.5
1502	S988	-3780	168.5
1503	S989	-3794	296.5
1504	S990	-3808	168.5
1505	S991	-3822	296.5
1506	S992	-3836	168.5
1507	S993	-3850	296.5
1508	S994	-3864	168.5
1509	S995	-3878	296.5
1510	S996	-3892	168.5
1511	S997	-3906	296.5
1512	S998	-3920	168.5
1513	S999	-3934	296.5
1514	S100	-3948	168.5
1515	S100	-3962	296.5
1516	S100	-3976	168.5
1517	S100	-3990	296.5
1518	S100	-4004	168.5
1519	S100	-4018	296.5
1520	S100	-4032	168.5
1521	S100	-4046	296.5
1522	S100	-4060	168.5
1523	S100	-4074	296.5
1524	S101	-4088	168.5
1525	S101	-4102	296.5
1526	S101	-4116	168.5
1527	S101	-4130	296.5
1528	S101	-4144	168.5
1529	S101	-4158	296.5
1530	S101	-4172	168.5
1531	S101	-4186	296.5
1532	S101	-4200	168.5
1533	S101	-4214	296.5
1534	S102	-4228	168.5
1535	S102	-4242	296.5
1536	S102	-4256	168.5
1537	S102	-4270	296.5
1538	S102	-4284	168.5
1539	S102	-4298	296.5
1540	S102	-4312	168.5
1541	S102	-4326	296.5
1542	S102	-4340	168.5
1543	S102	-4354	296.5
1544	S103	-4368	168.5
1545	S103	-4382	296.5
1546	S103	-4396	168.5
1547	S103	-4410	296.5
1548	S103	-4424	168.5
1549	S103	-4438	296.5
1550	S103	-4452	168.5

No.	Pad	X	Y
1551	S1037	-4466	296.5
1552	S1038	-4480	168.5
1553	S1039	-4494	296.5
1554	S1040	-4508	168.5
1555	S1041	-4522	296.5
1556	S1042	-4536	168.5
1557	S1043	-4550	296.5
1558	S1044	-4564	168.5
1559	S1045	-4578	296.5
1560	S1046	-4592	168.5
1561	S1047	-4606	296.5
1562	S1048	-4620	168.5
1563	S1049	-4634	296.5
1564	S1050	-4648	168.5
1565	S1051	-4662	296.5
1566	S1052	-4676	168.5
1567	S1053	-4690	296.5
1568	S1054	-4704	168.5
1569	S1055	-4718	296.5
1570	S1056	-4732	168.5
1571	S1057	-4746	296.5
1572	S1058	-4760	168.5
1573	S1059	-4774	296.5
1574	S1060	-4788	168.5
1575	S1061	-4802	296.5
1576	S1062	-4816	168.5
1577	S1063	-4830	296.5
1578	S1064	-4844	168.5
1579	S1065	-4858	296.5
1580	S1066	-4872	168.5
1581	S1067	-4886	296.5
1582	S1068	-4900	168.5
1583	S1069	-4914	296.5
1584	S1070	-4928	168.5
1585	S1071	-4942	296.5
1586	S1072	-4956	168.5
1587	S1073	-4970	296.5
1588	S1074	-4984	168.5
1589	S1075	-4998	296.5
1590	S1076	-5012	168.5
1591	S1077	-5026	296.5
1592	S1078	-5040	168.5
1593	S1079	-5054	296.5
1594	S1080	-5068	168.5
1595	S1081	-5082	296.5
1596	S1082	-5096	168.5
1597	S1083	-5110	296.5
1598	S1084	-5124	168.5
1599	S1085	-5138	296.5
1600	S1086	-5152	168.5

No.	Pad	X	Y
1601	S1087	-5166	296.5
1602	S1088	-5180	168.5
1603	S1089	-5194	296.5
1604	S1090	-5208	168.5
1605	S1091	-5222	296.5
1606	S1092	-5236	168.5
1607	S1093	-5250	296.5
1608	S1094	-5264	168.5
1609	S1095	-5278	296.5
1610	S1096	-5292	168.5
1611	S1097	-5306	296.5
1612	S1098	-5320	168.5
1613	S1099	-5334	296.5
1614	S1100	-5348	168.5
1615	S1101	-5362	296.5
1616	S1102	-5376	168.5
1617	S1103	-5390	296.5
1618	S1104	-5404	168.5
1619	S1105	-5418	296.5
1620	S1106	-5432	168.5
1621	S1107	-5446	296.5
1622	S1108	-5460	168.5
1623	S1109	-5474	296.5
1624	S1110	-5488	168.5
1625	S1111	-5502	296.5
1626	S1112	-5516	168.5
1627	S1113	-5530	296.5
1628	S1114	-5544	168.5
1629	S1115	-5558	296.5
1630	S1116	-5572	168.5
1631	S1117	-5586	296.5
1632	S1118	-5600	168.5
1633	S1119	-5614	296.5
1634	S1120	-5628	168.5
1635	S1121	-5642	296.5
1636	S1122	-5656	168.5
1637	S1123	-5670	296.5
1638	S1124	-5684	168.5
1639	S1125	-5698	296.5
1640	S1126	-5712	168.5
1641	S1127	-5726	296.5
1642	S1128	-5740	168.5
1643	S1129	-5754	296.5
1644	S1130	-5768	168.5
1645	S1131	-5782	296.5
1646	S1132	-5796	168.5
1647	S1133	-5810	296.5
1648	S1134	-5824	168.5
1649	S1135	-5838	296.5
1650	S1136	-5852	168.5

No.	Pad	X	Y
1651	S113	-5866	296.5
1652	S113	-5880	168.5
1653	S113	-5894	296.5
1654	S114	-5908	168.5
1655	S114	-5922	296.5
1656	S114	-5936	168.5
1657	S114	-5950	296.5
1658	S114	-5964	168.5
1659	S114	-5978	296.5
1660	S114	-5992	168.5
1661	S114	-6006	296.5
1662	S114	-6020	168.5
1663	S114	-6034	296.5
1664	S115	-6048	168.5
1665	S115	-6062	296.5
1666	S115	-6076	168.5
1667	S115	-6090	296.5
1668	S115	-6104	168.5
1669	S115	-6118	296.5
1670	S115	-6132	168.5
1671	S115	-6146	296.5
1672	S115	-6160	168.5
1673	S115	-6174	296.5
1674	S116	-6188	168.5
1675	S116	-6202	296.5
1676	S116	-6216	168.5
1677	S116	-6230	296.5
1678	S116	-6244	168.5
1679	S116	-6258	296.5
1680	S116	-6272	168.5
1681	S116	-6286	296.5
1682	S116	-6300	168.5
1683	S116	-6314	296.5
1684	S117	-6328	168.5
1685	S117	-6342	296.5
1686	S117	-6356	168.5
1687	S117	-6370	296.5
1688	S117	-6384	168.5
1689	S117	-6398	296.5
1690	S117	-6412	168.5
1691	S117	-6426	296.5
1692	S117	-6440	168.5
1693	S117	-6454	296.5
1694	S118	-6468	168.5
1695	S118	-6482	296.5
1696	S118	-6496	168.5
1697	S118	-6510	296.5
1698	S118	-6524	168.5
1699	S118	-6538	296.5
1700	S118	-6552	168.5

No.	Pad	X	Y
1701	S1187	-6566	296.5
1702	S1188	-6580	168.5
1703	S1189	-6594	296.5
1704	S1190	-6608	168.5
1705	S1191	-6622	296.5
1706	S1192	-6636	168.5
1707	S1193	-6650	296.5
1708	S1194	-6664	168.5
1709	S1195	-6678	296.5
1710	S1196	-6692	168.5
1711	S1197	-6706	296.5
1712	S1198	-6720	168.5
1713	S1199	-6734	296.5
1714	S1200	-6748	168.5
1715	S1201	-6762	296.5
1716	S1202	-6776	168.5
1717	S1203	-6790	296.5
1718	S1204	-6804	168.5
1719	S1205	-6818	296.5
1720	S1206	-6832	168.5
1721	S1207	-6846	296.5
1722	S1208	-6860	168.5
1723	S1209	-6874	296.5
1724	S1210	-6888	168.5
1725	S1211	-6902	296.5
1726	S1212	-6916	168.5
1727	S1213	-6930	296.5
1728	S1214	-6944	168.5
1729	S1215	-6958	296.5
1730	S1216	-6972	168.5
1731	S1217	-6986	296.5
1732	S1218	-7000	168.5
1733	S1219	-7014	296.5
1734	S1220	-7028	168.5
1735	S1221	-7042	296.5
1736	S1222	-7056	168.5
1737	S1223	-7070	296.5
1738	S1224	-7084	168.5
1739	S1225	-7098	296.5
1740	S1226	-7112	168.5
1741	S1227	-7126	296.5
1742	S1228	-7140	168.5
1743	S1229	-7154	296.5
1744	S1230	-7168	168.5
1745	S1231	-7182	296.5
1746	S1232	-7196	168.5
1747	S1233	-7210	296.5
1748	S1234	-7224	168.5
1749	S1235	-7238	296.5
1750	S1236	-7252	168.5

No.	Pad	X	Y
1751	S1237	-7266	296.5
1752	S1238	-7280	168.5
1753	S1239	-7294	296.5
1754	S1240	-7308	168.5
1755	S1241	-7322	296.5
1756	S1242	-7336	168.5
1757	S1243	-7350	296.5
1758	S1244	-7364	168.5
1759	S1245	-7378	296.5
1760	S1246	-7392	168.5
1761	S1247	-7406	296.5
1762	S1248	-7420	168.5
1763	S1249	-7434	296.5
1764	S1250	-7448	168.5
1765	S1251	-7462	296.5
1766	S1252	-7476	168.5
1767	S1253	-7490	296.5
1768	S1254	-7504	168.5
1769	S1255	-7518	296.5
1770	S1256	-7532	168.5
1771	S1257	-7546	296.5
1772	S1258	-7560	168.5
1773	S1259	-7574	296.5
1774	S1260	-7588	168.5
1775	S1261	-7602	296.5
1776	S1262	-7616	168.5
1777	S1263	-7630	296.5
1778	S1264	-7644	168.5
1779	S1265	-7658	296.5
1780	S1266	-7672	168.5
1781	S1267	-7686	296.5
1782	S1268	-7700	168.5
1783	S1269	-7714	296.5
1784	S1270	-7728	168.5
1785	S1271	-7742	296.5
1786	S1272	-7756	168.5
1787	S1273	-7770	296.5
1788	S1274	-7784	168.5
1789	S1275	-7798	296.5
1790	S1276	-7812	168.5
1791	S1277	-7826	296.5
1792	S1278	-7840	168.5
1793	S1279	-7854	296.5
1794	S1280	-7868	168.5
1795	S1281	-7882	296.5
1796	S1282	-7896	168.5
1797	S1283	-7910	296.5
1798	S1284	-7924	168.5
1799	S1285	-7938	296.5
1800	S1286	-7952	168.5

No.	Pad	X	Y
1801	S128	-7966	296.5
1802	S128	-7980	168.5
1803	S128	-7994	296.5
1804	S129	-8008	168.5
1805	S129	-8022	296.5
1806	S129	-8036	168.5
1807	S129	-8050	296.5
1808	S129	-8064	168.5
1809	S129	-8078	296.5
1810	S129	-8092	168.5
1811	S129	-8106	296.5
1812	S129	-8120	168.5
1813	S129	-8134	296.5
1814	S130	-8148	168.5
1815	S130	-8162	296.5
1816	S130	-8176	168.5
1817	S130	-8190	296.5
1818	S130	-8204	168.5
1819	S130	-8218	296.5
1820	S130	-8232	168.5
1821	S130	-8246	296.5
1822	S130	-8260	168.5
1823	S130	-8274	296.5
1824	S131	-8288	168.5
1825	S131	-8302	296.5
1826	S131	-8316	168.5
1827	S131	-8330	296.5
1828	S131	-8344	168.5
1829	S131	-8358	296.5
1830	S131	-8372	168.5
1831	S131	-8386	296.5
1832	S131	-8400	168.5
1833	S131	-8414	296.5
1834	S132	-8428	168.5
1835	S132	-8442	296.5
1836	S132	-8456	168.5
1837	S132	-8470	296.5
1838	S132	-8484	168.5
1839	S132	-8498	296.5
1840	S132	-8512	168.5
1841	S132	-8526	296.5
1842	S132	-8540	168.5
1843	S132	-8554	296.5
1844	S133	-8568	168.5
1845	S133	-8582	296.5
1846	S133	-8596	168.5
1847	S133	-8610	296.5
1848	S133	-8624	168.5
1849	S133	-8638	296.5
1850	S133	-8652	168.5
1851	S1337	-8666	296.5
1852	S1338	-8680	168.5
1853	S1339	-8694	296.5
1854	S1340	-8708	168.5
1855	S1341	-8722	296.5
1856	S1342	-8736	168.5
1857	S1343	-8750	296.5
1858	S1344	-8764	168.5
1859	S1345	-8778	296.5
1860	S1346	-8792	168.5
1861	S1347	-8806	296.5
1862	S1348	-8820	168.5
1863	S1349	-8834	296.5
1864	S1350	-8848	168.5
1865	S1351	-8862	296.5
1866	S1352	-8876	168.5
1867	S1353	-8890	296.5
1868	S1354	-8904	168.5
1869	S1355	-8918	296.5
1870	S1356	-8932	168.5
1871	S1357	-8946	296.5
1872	S1358	-8960	168.5
1873	S1359	-8974	296.5
1874	S1360	-8988	168.5
1875	S1361	-9002	296.5
1876	S1362	-9016	168.5
1877	S1363	-9030	296.5
1878	S1364	-9044	168.5
1879	S1365	-9058	296.5
1880	S1366	-9072	168.5
1881	S1367	-9086	296.5
1882	S1368	-9100	168.5
1883	S1369	-9114	296.5
1884	S1370	-9128	168.5
1885	S1371	-9142	296.5
1886	S1372	-9156	168.5
1887	S1373	-9170	296.5
1888	S1374	-9184	168.5
1889	S1375	-9198	296.5
1890	S1376	-9212	168.5
1891	S1377	-9226	296.5
1892	S1378	-9240	168.5
1893	S1379	-9254	296.5
1894	S1380	-9268	168.5
1895	S1381	-9282	296.5
1896	S1382	-9296	168.5
1897	S1383	-9310	296.5
1898	S1384	-9324	168.5
1899	S1385	-9338	296.5
1900	S1386	-9352	168.5
1901	S1387	-9366	296.5
1902	S1388	-9380	168.5
1903	S1389	-9394	296.5
1904	S1390	-9408	168.5
1905	S1391	-9422	296.5
1906	S1392	-9436	168.5
1907	S1393	-9450	296.5
1908	S1394	-9464	168.5
1909	S1395	-9478	296.5
1910	S1396	-9492	168.5
1911	S1397	-9506	296.5
1912	S1398	-9520	168.5
1913	S1399	-9534	296.5
1914	S1400	-9548	168.5
1915	S1401	-9562	296.5
1916	S1402	-9576	168.5
1917	S1403	-9590	296.5
1918	S1404	-9604	168.5
1919	S1405	-9618	296.5
1920	S1406	-9632	168.5
1921	S1407	-9646	296.5
1922	S1408	-9660	168.5
1923	S1409	-9674	296.5
1924	S1410	-9688	168.5
1925	S1411	-9702	296.5
1926	S1412	-9716	168.5
1927	S1413	-9730	296.5
1928	S1414	-9744	168.5
1929	S1415	-9758	296.5
1930	S1416	-9772	168.5
1931	S1417	-9786	296.5
1932	S1418	-9800	168.5
1933	S1419	-9814	296.5
1934	S1420	-9828	168.5
1935	S1421	-9842	296.5
1936	S1422	-9856	168.5
1937	S1423	-9870	296.5
1938	S1424	-9884	168.5
1939	S1425	-9898	296.5
1940	S1426	-9912	168.5
1941	S1427	-9926	296.5
1942	S1428	-9940	168.5
1943	S1429	-9954	296.5
1944	S1430	-9968	168.5
1945	S1431	-9982	296.5
1946	S1432	-9996	168.5
1947	S1433	-1001	296.5
1948	S1434	-1002	168.5
1949	S1435	-1003	296.5
1950	S1436	-1005	168.5

No.	Pad	X	Y
1951	S143	-10066	296.5
1952	S143	-10080	168.5
1953	S143	-10094	296.5
1954	S144	-10108	168.5
1955	SDU	-10122	296.5
1956	VGLO	-10220	168.5
1957	VGLO	-10234	296.5
1958	VGLO	-10248	168.5
1959	VGLO	-10262	296.5
1960	VGLO	-10276	168.5
1961	VGLO	-10296.	296.5
1962	VGH	-10304	168.5
1963	VGH	-10318	296.5
1964	VGH	-10332	168.5
1965	VGH	-10346	296.5
1966	VGH	-10360	168.5
1967	VGH	-10374	296.5
1968	VGH	-10388	168.5
1969	VGH	-10402	296.5
1970	VSSI	-10416	168.5
1971	VSSI	-10430	296.5
1972	VSSI	-10444	168.5
1973	VSSI	-10458	296.5
1974	VSSI	-10472	168.5
1975	VSSI	-10486	296.5
1976	VSSI	-10500	168.5
1977	VSSI	-10514	296.5
1978	VSSI	-10528	168.5
1979	VSSI	-10542	296.5
1980	VSSI	-10556	168.5
1981	VSSI	-10570	296.5
1982	VSSI	-10584	168.5
1983	VSSI	-10598	296.5
1984	VSSI	-10612	168.5
1985	VSSI	-10626	296.5
1986	VSSI	-10640	168.5
1987	VSSI	-10654	296.5
1988	VSSI	-10668	168.5
1989	VSSI	-10682	296.5
1990	VSSI	-10696	168.5
1991	VSSI	-10710	296.5
1992	VSSI	-10724	168.5
1993	VSSI	-10738	296.5
1994	VSSI	-10752	168.5
1995	VSSI	-10766	296.5
1996	VSSI	-10780	168.5
1997	VSSI	-10794	296.5
1998	VSSI	-10808	168.5
1999	VSSI	-10822	296.5
2000	VSSI	-10836	168.5

No.	Pad	X	Y
2001	VSSIDU	-1085	296.5
2002	VSSIDU	-1086	168.5
2003	VSSIDU	-1087	296.5
2004	VSSIDU	-1089	168.5
2005	VSSIDU	-1090	296.5
2006	VSSIDU	-1092	168.5
2007	VSSIDU	-1093	296.5
2008	VSSIDU	-1094	168.5
2009	VSSIDU	-1096	296.5
2010	VSSIDU	-1097	168.5
2011	VSSIDU	-1099	296.5
2012	VSSIDU	-1100	168.5
2013	VSSIDU	-1101	296.5
2014	GOUT17	-1103	168.5
2015	GOUT17	-1104	296.5
2016	GOUT18	-1106	168.5
2017	GOUT18	-1107	296.5
2018	GOUT19	-1108	168.5
2019	GOUT19	-1110	296.5
2020	GOUT20	-1111	168.5
2021	GOUT20	-1113	296.5
2022	GOUT21	-1114	168.5
2023	GOUT21	-1115	296.5
2024	GOUT22	-1117	168.5
2025	GOUT22	-1118	296.5
2026	GOUT23	-1120	168.5
2027	GOUT23	-1121	296.5
2028	GOUT24	-1122	168.5
2029	GOUT24	-1124	296.5
2030	GOUT25	-1125	168.5
2031	GOUT25	-1127	296.5
2032	GOUT26	-1128	168.5
2033	GOUT26	-1129	296.5
2034	GOUT27	-1131	168.5
2035	GOUT27	-1132	296.5
2036	GOUT28	-1134	168.5
2037	GOUT28	-1135	296.5
2038	GOUT29	-1136	168.5
2039	GOUT29	-1138	296.5
2040	GOUT30	-1139	168.5
2041	GOUT30	-1141	296.5
2042	GOUT_V	-1142	168.5
2043	GOUT_V	-1143	296.5
2044	VGLO	-1145	168.5
2045	VRGH	-1146	296.5
2046	VRGH	-1148	168.5
2047	VRGH	-1149	296.5
2048	LVGL	-1150	168.5
2049	LVGL	-1152	296.5
2050	LVGL	-1153	168.5

No.	Pad	X	Y
2051	GOUT31	-1155	296.5
2052	GOUT31	-1156	168.5
2053	GOUT32	-1157	296.5
2054	GOUT32	-1159	168.5
2055	GOUT_VGL	-1160	296.5
2056	GOUT_VGL	-1162	168.5
2057	GOUT_VGL	-1163	296.5
2058	VGHO	-1164	168.5
2059	VGHO	-1166	296.5
2060	VGHO	-1167	168.5
2061	DUMMY	-1169	296.5
2062	DUMMY	-1170	168.5
2063	DUMMY	-1171	296.5
2064	DUMMY	-1173	168.5
2065	DUMMY	-1176	296.5

5 System Interface

5.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in **Table 5.1.1**

Table 5.1.1 Interface Type Selection

IM3	IM2	IM1	IM0	Display Data	Register
1	0	0	1	RGB interface, D[23:0]	8-bit SPI, SDI/SDO serial data, SCL rising trigger
0	0	0	1	RGB interface, D[23:0]	8-bit SPI, SDI/SDO serial data, SCL falling trigger
1	0	1	0	RGB interface, D[23:0]	9-bit SPI, SDI/SDO serial data, SCL rising trigger
0	0	1	0	RGB interface, D[23:0]	9-bit SPI, SDI/SDO serial data, SCL falling trigger
0	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL falling trigger
x	1	0	1	MIPI DSI, D0_P/N, D1_P/N	MIPI DSI, D0_P/N, D1_P/N

5.2 SPI Interface

The following is selection of interface decided by the IM [3:0] pins.

The GC9503NP uses a 3-line 9-bit serial interface for communication between the host and the GC9503NP. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the data transfer of DPI interface, the unused pins are unaffected. The Serial clock (SCL) is used only for the interface with the MPU, so it can be stopped when no communication is necessary.

5.2.1 SPI-8BIT/9BIT Write Cycle Sequence

In write mode of the interface, the host writes commands and data to the GC9503NP. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is “low”, the transmission byte is interpreted as a command byte. If the D/C bit is “high”, the transmission byte is stored in the command register as a parameter data.

Any instruction can be sent in any order to the GC9503NP and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data are ineffective. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-line serial interface.

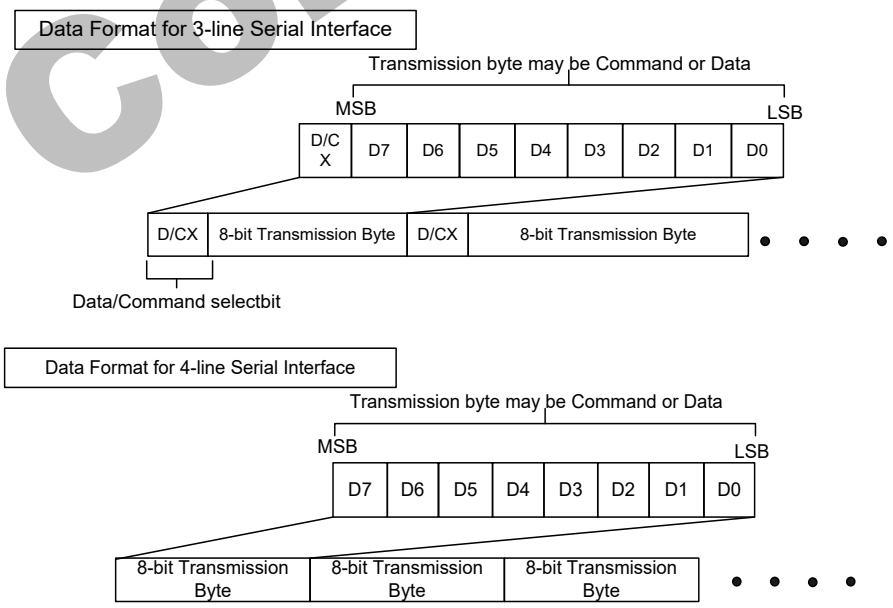


Figure 2 DBI data format

The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the GC9503NP on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the

optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences described in the Figure 3 below

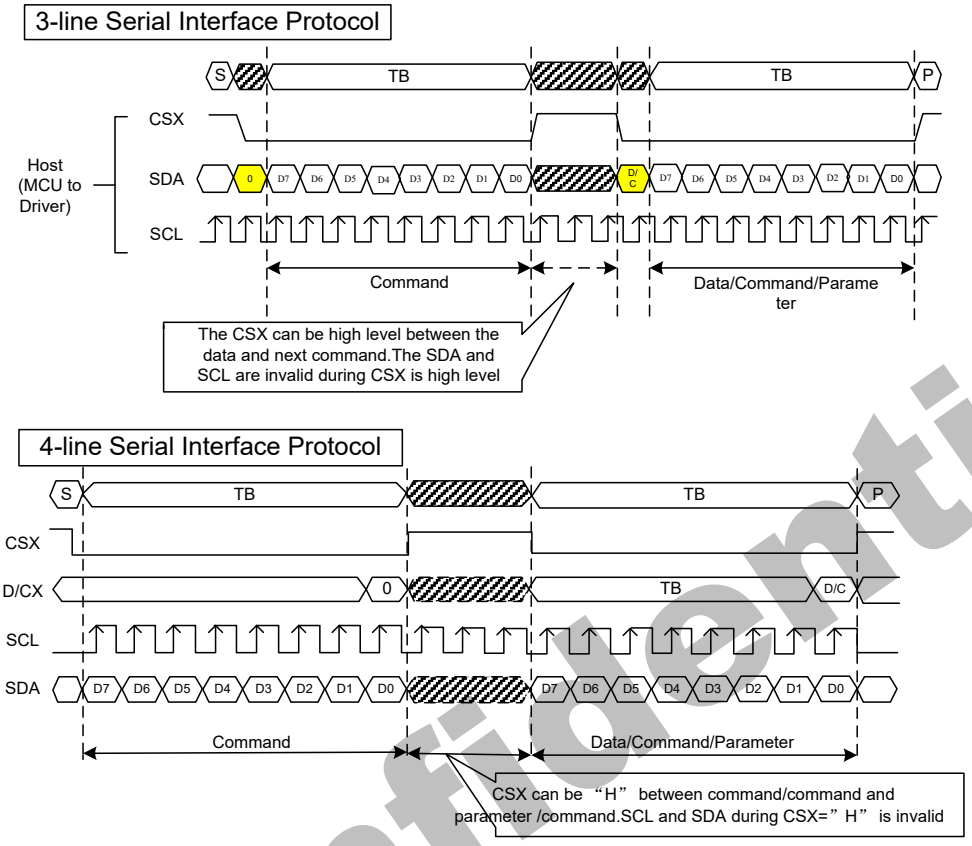


Figure 3 SPI protocol (SCL rising edge example)

5.2.2 SPI-8BIT/9BIT Read Cycle Sequence

In read mode of the interface, the host reads the register value from the GC9503NP. The host sends a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The GC9503NP samples the SDI (input data) at the rising edges of the SCL (serial clock), and shifts SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

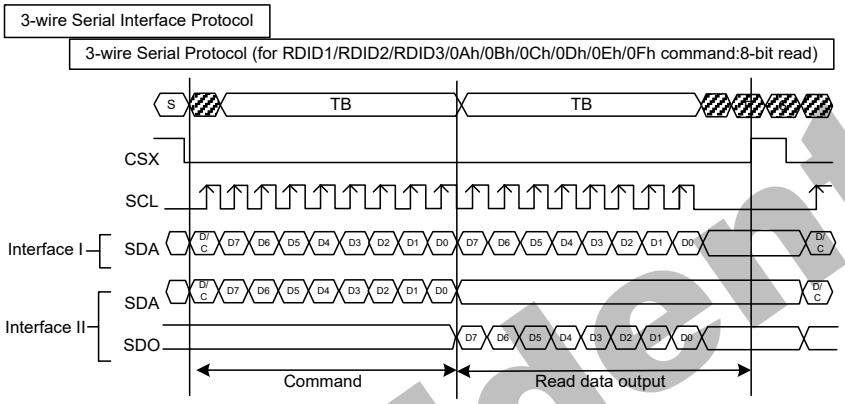


Figure 4 SPI read cycle sequence (SCL rising edge example)

5.2.3 Data Transfer Break and Recovery

If there data transmission is broken by CSX pulse while transferring a Command, Multiple parameter command, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

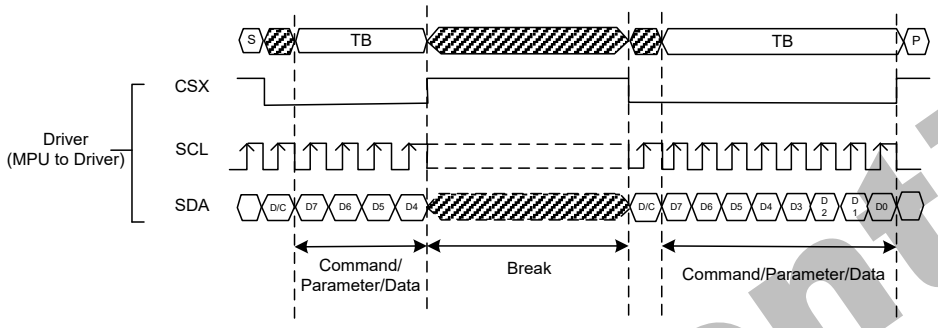


Figure 5 Data Transfer Break and Recovery (SCL rising edge example)

If there is a break in data transmission of a multiple parameter command, and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below. See diagram

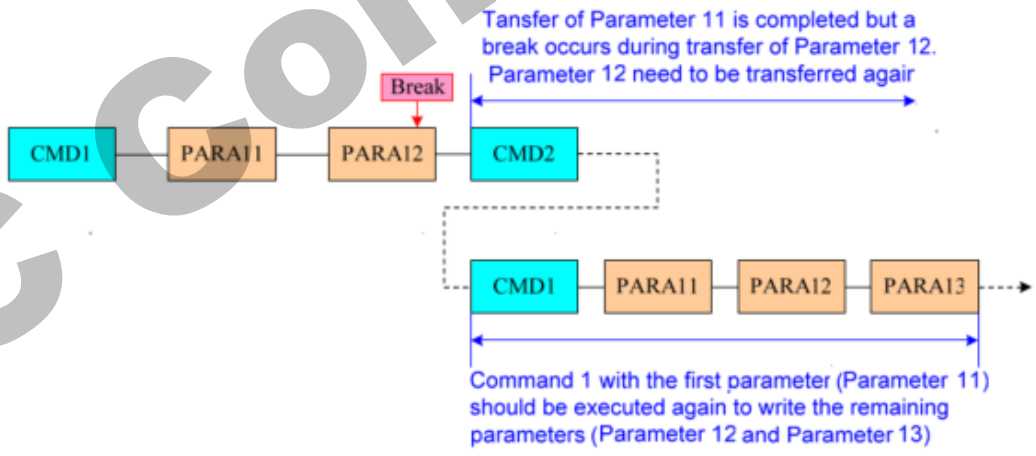


Figure 6 Data Transfer Break -Case 1

If a multiple parameter command is sent and a break occurs when a new command is sent before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command remain at the previous value.

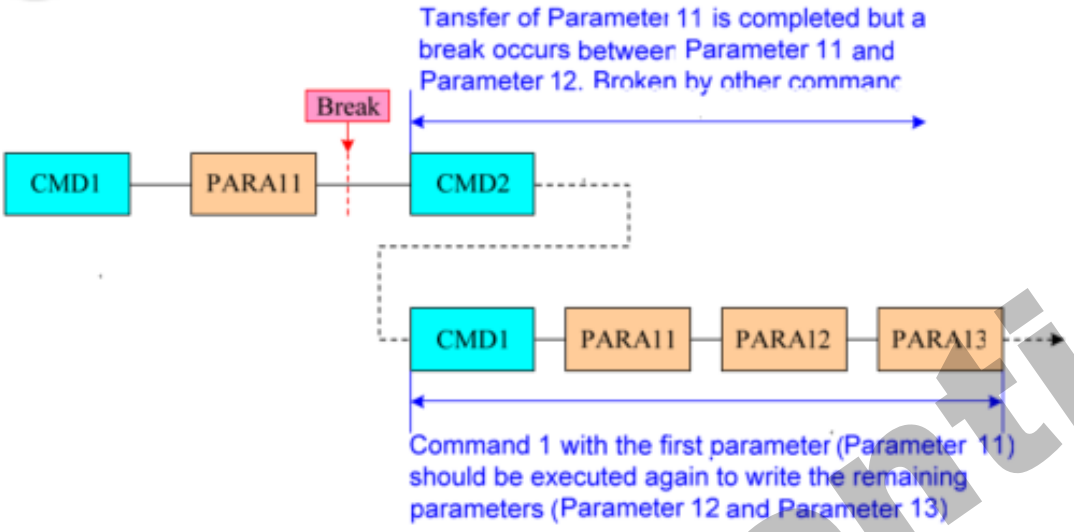


Figure 7 Data Transfer Break -Case 2

5.3 DPI (RGB) Interface

5.3.1 DPI Interface Selection

The DPI interface is operated with VS, HS, DE PCLK, DB [23:0] lines. It supports several pixel formats that can be selected by DPI [2:0] bits in “Pixel Format Set (R3Ah)” of Page 0 command. The selection of a given interface is defined by DPI [2:0] as show in the Table 9 and Figure 10 below.

Table 9 DPI (RGB) Interface Selection

DPI [2:0]			DPI (RGB) Interface	Used Pins
1	0	1	16-bit RGB interface	VS, HS, DE, PCLK,DB [20:16] , DB [13:8],
1	1	0	18-bit RGB interface	VS, HS, DE, PCLK, DB [21:16] , DB [13:8],
1	1	1	24-bit RGB interface	VS, HS, DE, PCLK, DB [23:0]
Others			Setting prohibited	

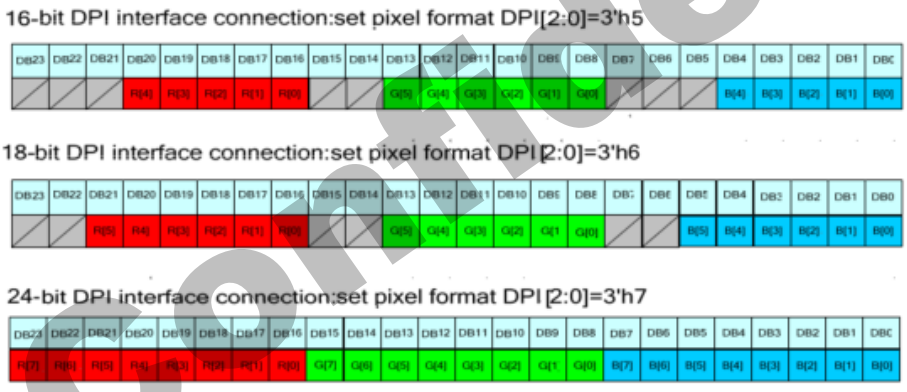


Figure 10 DPI (RGB) Interface 16/18/24-bit pixel format selection

The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and DB [23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical synchronization (Vsync) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. DB [23:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of PCLK). DB [23:0] can be ‘0’ (low) or ‘1’ (high). These lines

are read by a rising edge of the PCLK signal.

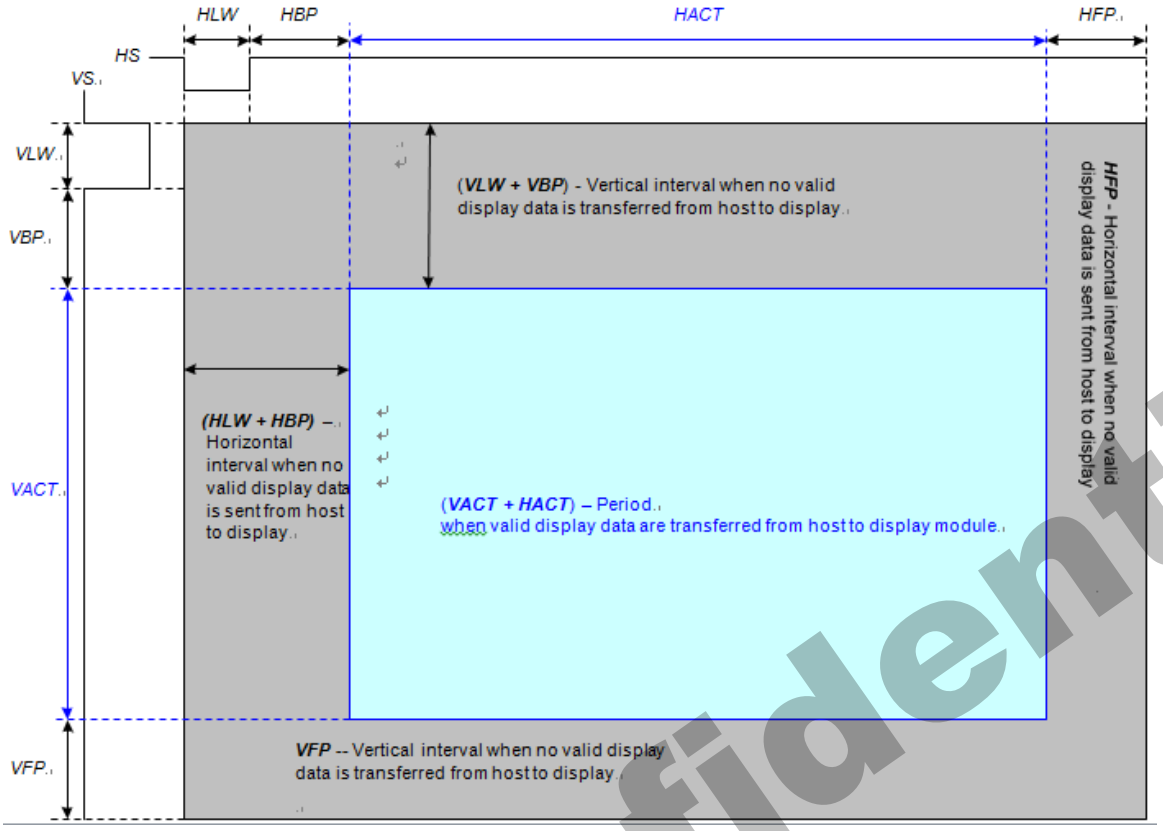
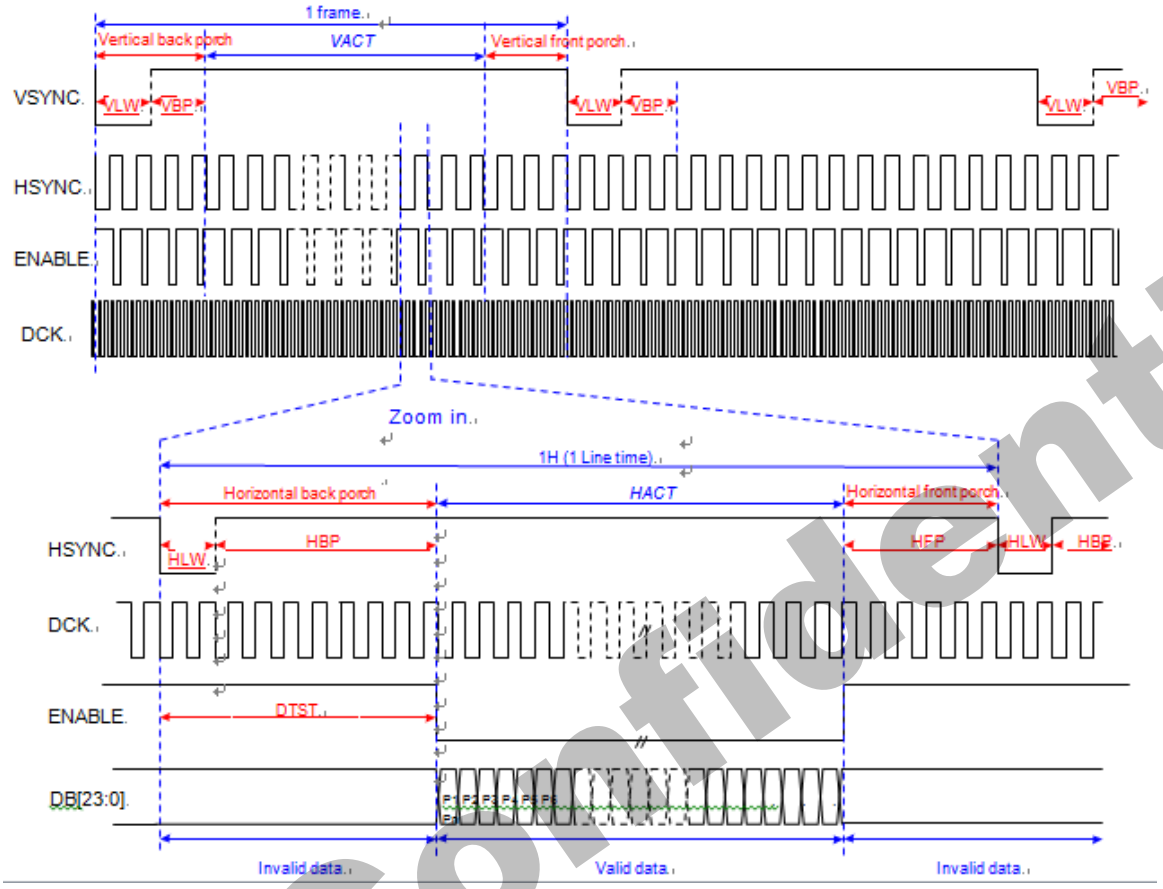


Figure 11 General DPI timing diagram

5.3.2 DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode is illustrated in Figure 12.



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2…, pixel n

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				960	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		35.7	MHz

Figure 12 DPI Interface Timing diagram

Note1. HLW+HBP+HFP >= 4.5us.
Note2. VSPL='0', HSPL='0', DPL='0' and EPL='0' of "(Interface Mode Control 21h of the Page 1)" command.

5.4 DSI system interface

5.4.1 General Description

The MIPI DSI is enabled or disabled by external IM[3:0] pin.

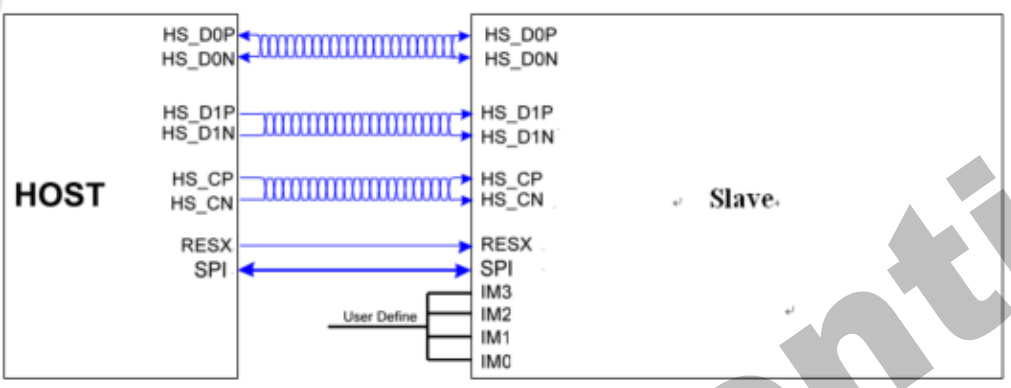


Figure 13 DSI system interface diagram

IM3	IM2	IM1	IM0	MPU Interface	Data Pin in Use
0	1	0	1	DSI interface	HS_CP, HS_CN, HS_D0P,HS_D0N, HS_D1P,HS_D1N,

The communication is separated into two different levels between the MPU and the display module:

Low level communication is done on the interface level.

High level communication is done on the packet level.

5.4.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode. High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 10 High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Note 1 Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

Note 2 If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Note 3 *n = 0 and 1 (D1+/- lanes only for HS-0 and HS-1)*

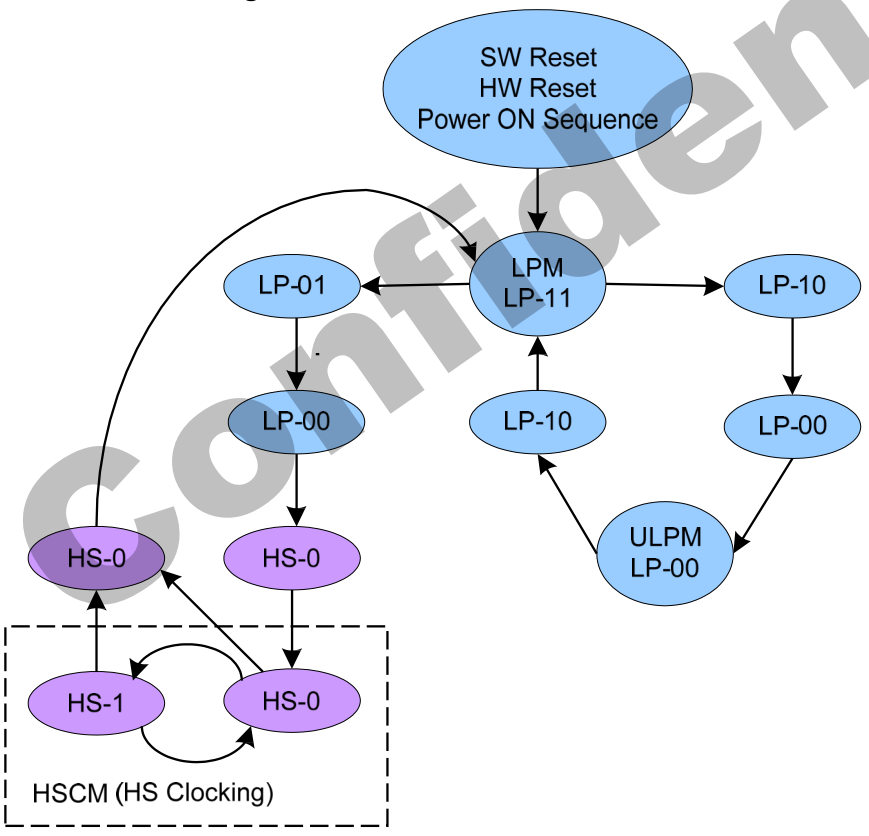
5.4.3 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

Figure 14 Clock Lanes Power Modes



5.4.4 Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

After SW Reset, HW Reset or Power On Sequence =>LP-11

After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM).

This sequence is illustrated below.

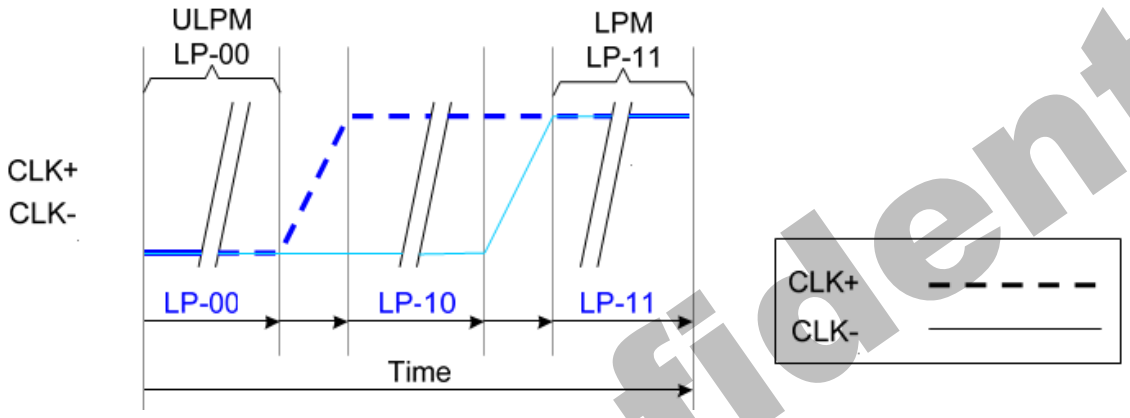


Figure 15 From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.

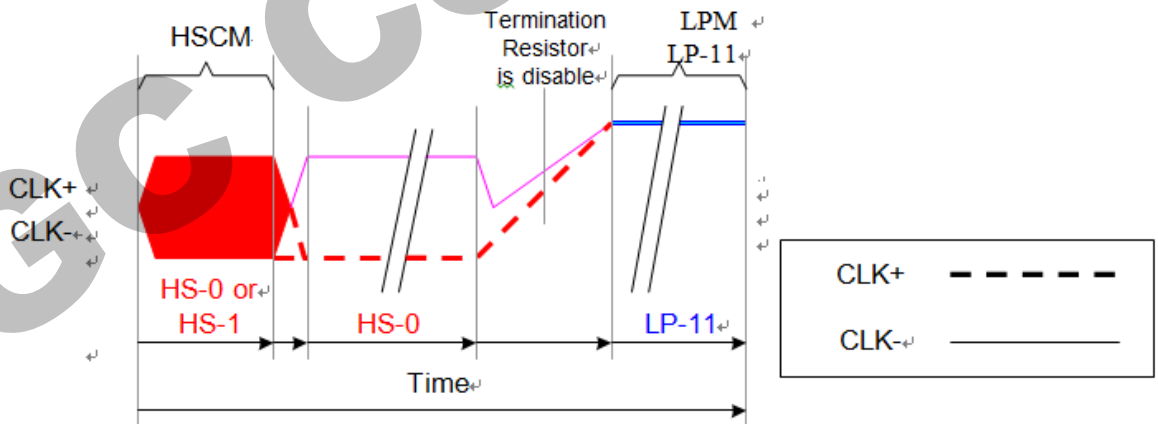


Figure 16 From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.

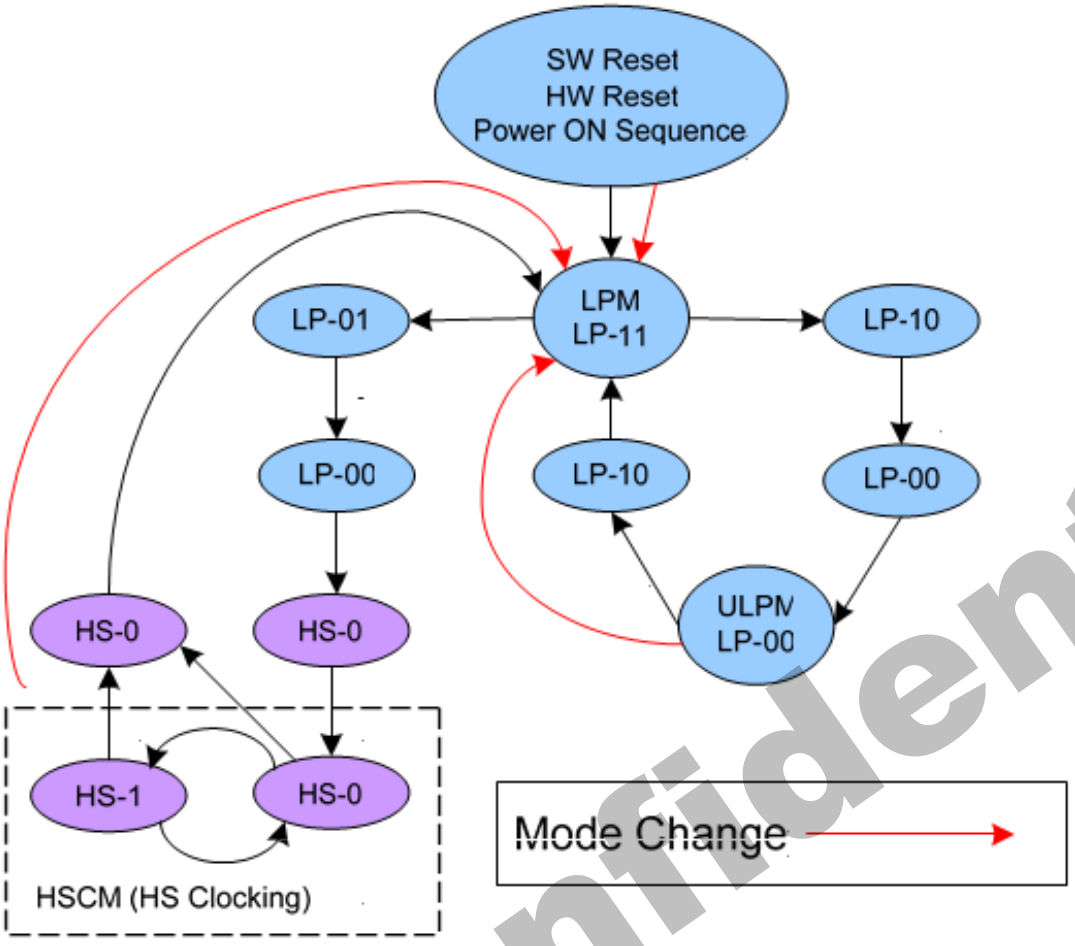


Figure 17 All Three Mode Changes to LPM on the Flow Chart

5.4.5 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10

=>LP-00 (ULPM).

This sequence is illustrated below.

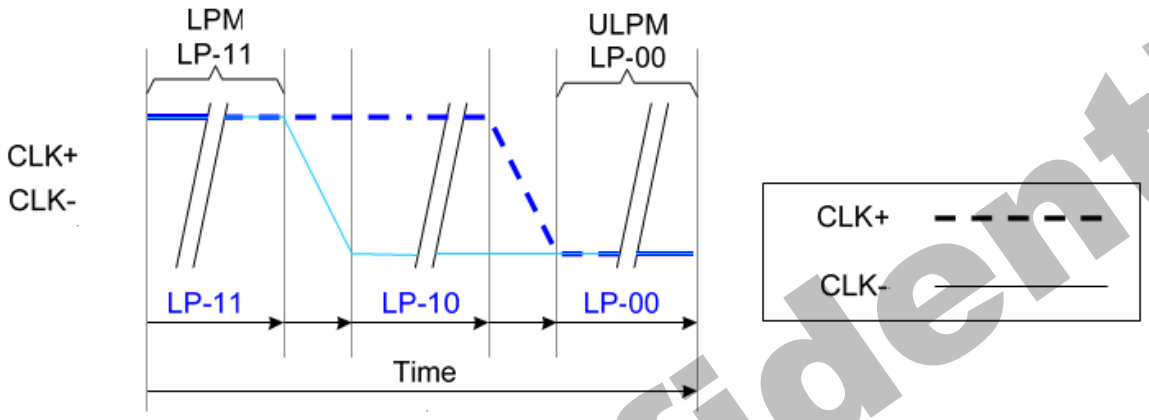


Figure 18 From LPM to ULPM

The mode change is also illustrated below.

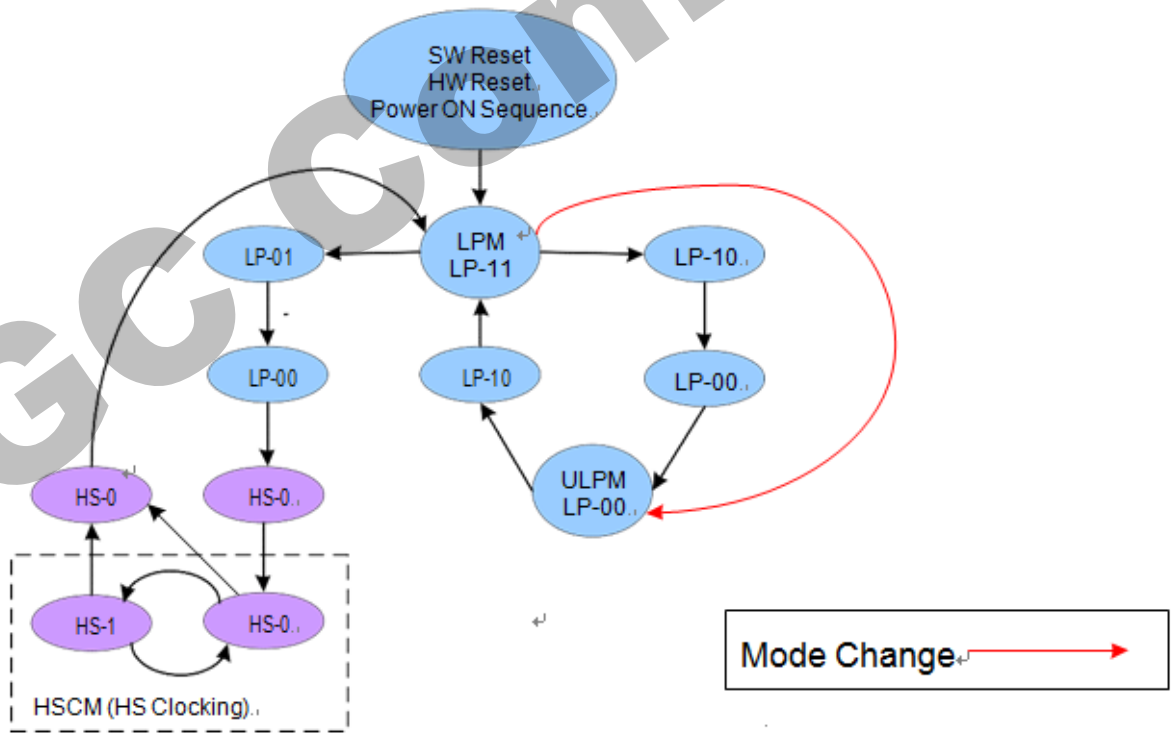


Figure 19 Mode Change from LPM to ULPM on the Flow Chart

5.4.6 High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

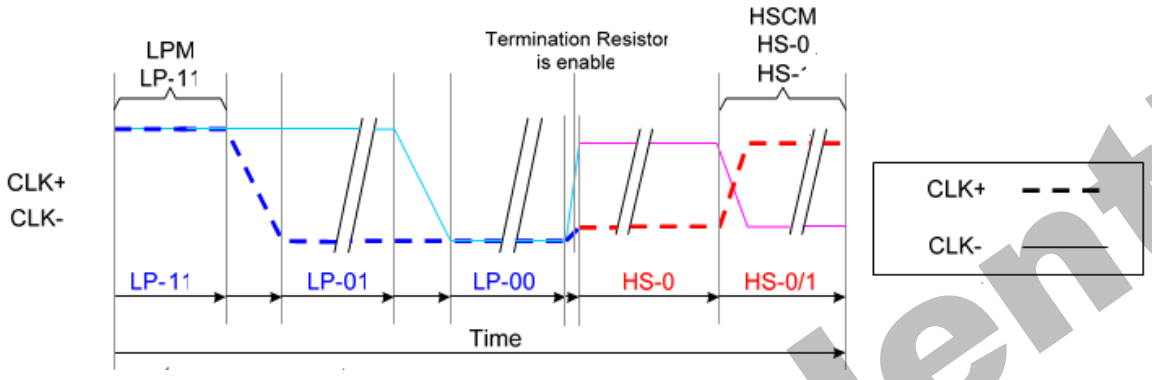


Figure 20 From LPM to HSCM

The mode change is also illustrated below.

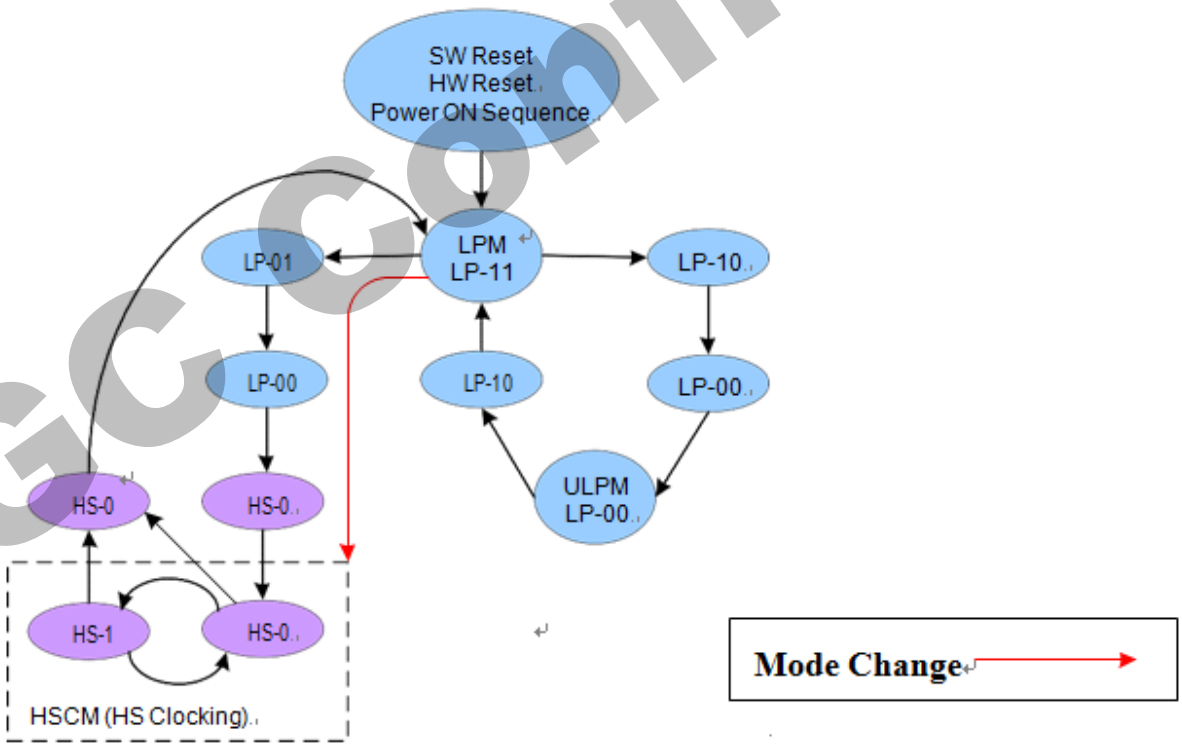


Figure 21 Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

Even number of transitions

Start state is HS-0

End state is HS-0

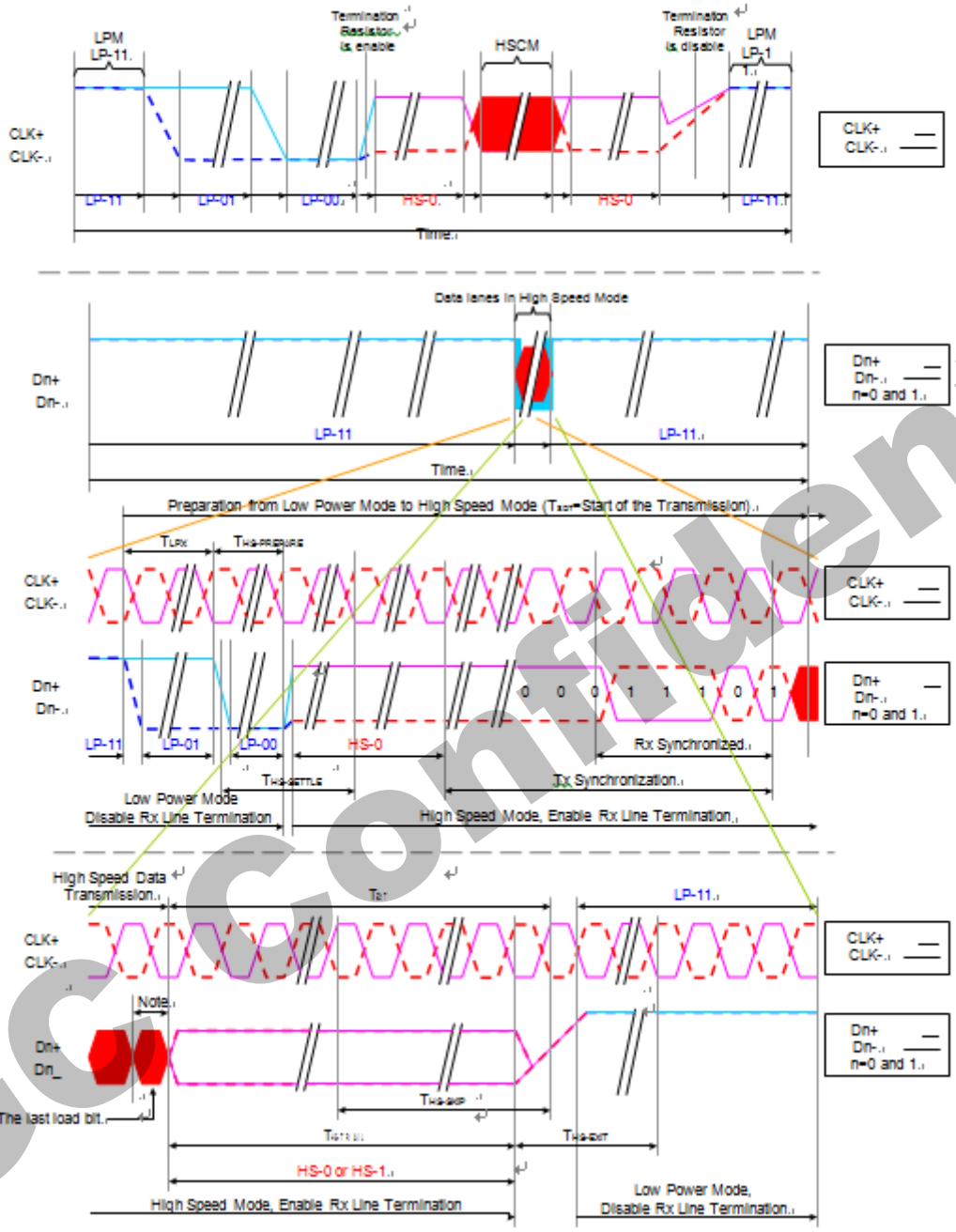


Figure 22 High Speed Clock Burst[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.4.7 DSI-D1 and DSI-D0 Data Lanes

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven in different modes which are:

Escape Mode (Only DSI-D0+/- data lanes are used)

High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)

Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 11 Entering and Leaving Sequences[Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 -+ LP-10 -+ LP-00 -+ LP-01 -+ LP-00	LP-00 -+ LP-10 -+ LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 -+ LP-01 -+ LP-00 -+ HS-0	(HS-0 or HS-1) -+ LP-11
Bus Turnaround Request	LP-11 -+ LP-10 -+ LP-00 -+ LP-10 -+ LP-00	Hi-Z

Note 1. DSI-D1+/- and DSI-D0+/- data lanes are used.
2. More information on chapter "Bus Turnaround ".

5.4.8 Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

Send “Low-Power Data Transmission” (LPDT) e.g. from the MPU to the display module,

Drive data lanes to “Ultra-Low Power State” (ULPS),

Indicate “Remote Application Reset” (RAR), which is resetting the display module,

Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follow

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0-= 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.

A load if it is needed

Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

End: LP-11

This basic construction is illustrated below:

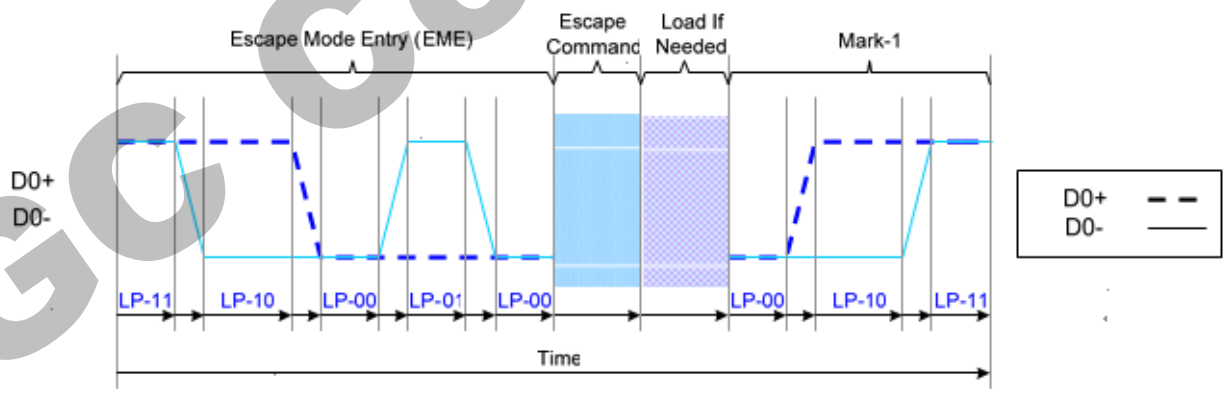


Figure 23 General Escape Mode Sequence

There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers, see Table 12: Escape Commands.

An example of a Mode type Escape Command is ‘Ultra-Low Power Mode’ where the MPU instructs the display module to enter it’s Ultra-Low Power Mode.

Escape commands are defined on the next table.

Table 12 Escape Commands[Note]

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Bit -+ Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1,note1	Mode	1001 1111 b	-	-
Undefined-2,note1	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, note1	Trigger	1010 0000 b	-	-

Note:This Escape command support has not been implemented on the display module.
n = 1
x = Supported
- = Not Supported

5.4.9 Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MPU.

The Low Power Data Transmission (LPDT) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

Load (Data):

One or more bytes (8 bit)

Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

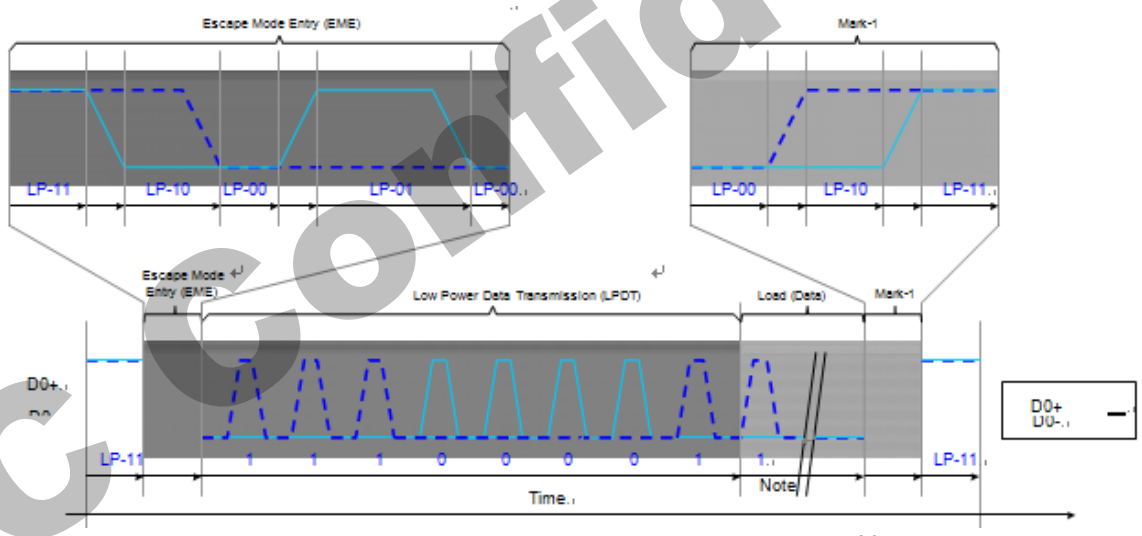


Figure 24 Low-Power Data Transmission (LPDT)N

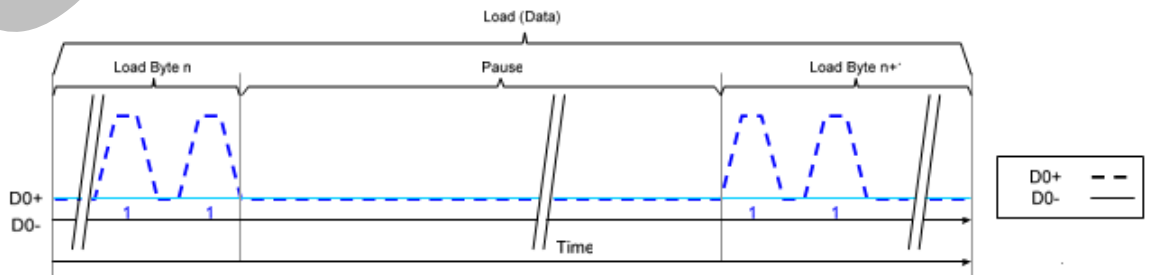


Figure 25 Pause (Example)

Note Load (Data) is presenting that the first bit is logical '1' in this example.

5.4.10 Ultra-Low Power State (ULPS)

The MPU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

Ultra-Low Power State (ULPS) when the MPU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

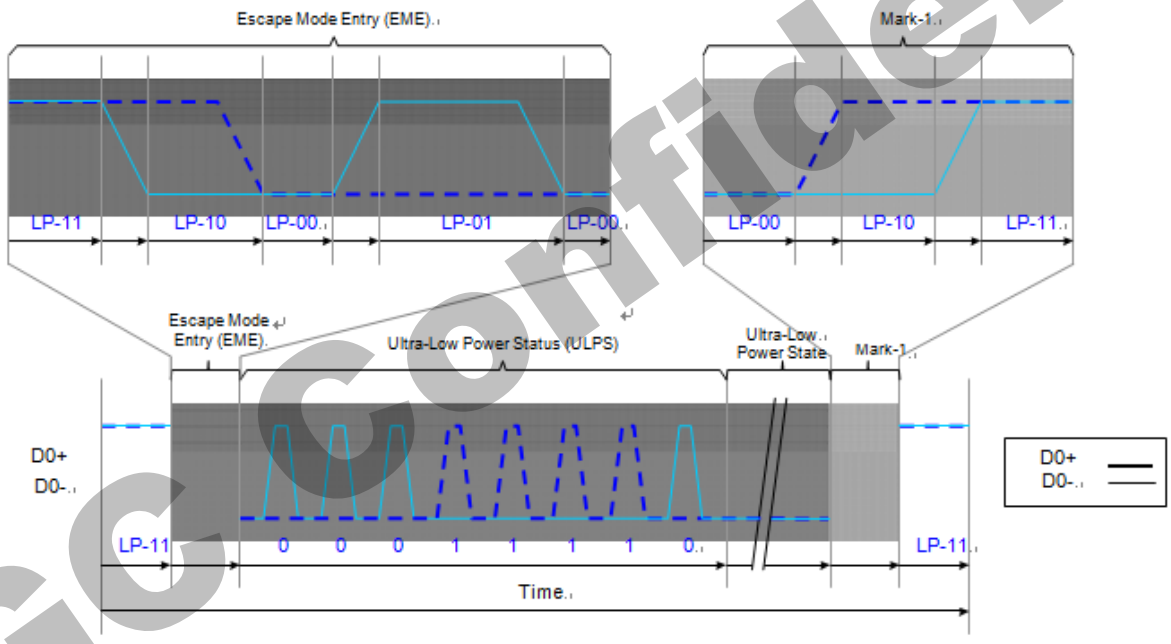


Figure 26 Ultra-Low Power State (ULPS)

5.4.11 Acknowledge (ACK)

The display module can inform to the MPU when an error has not recognized on it by Acknowledge (ACK). The display module is sending the Acknowledge (ACK) what is using a following sequence:

Start: LP-11

Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

End: LP-11

This sequence is illustrated for reference purposes below:

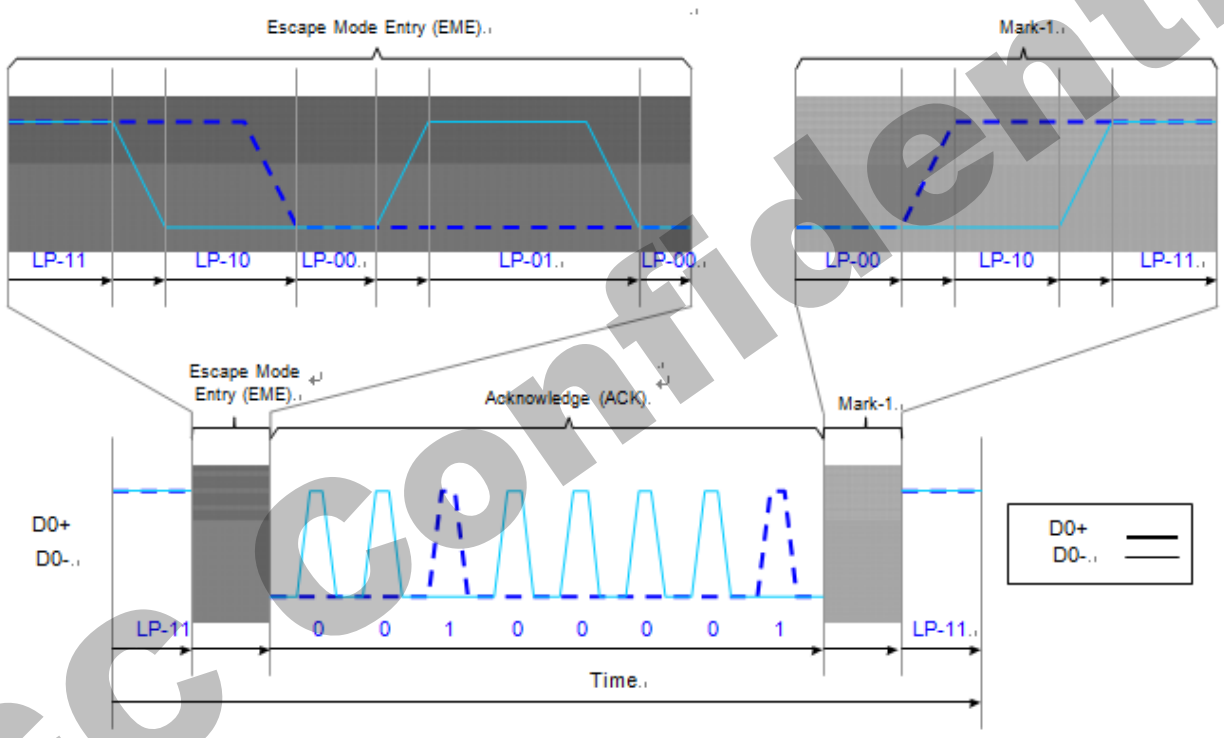


Figure 28 Acknowledge (ACK)

5.4.12 Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MPU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission (HSDT) as follows

Start: LP-11

HS-Request: LP-01

HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)

End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below

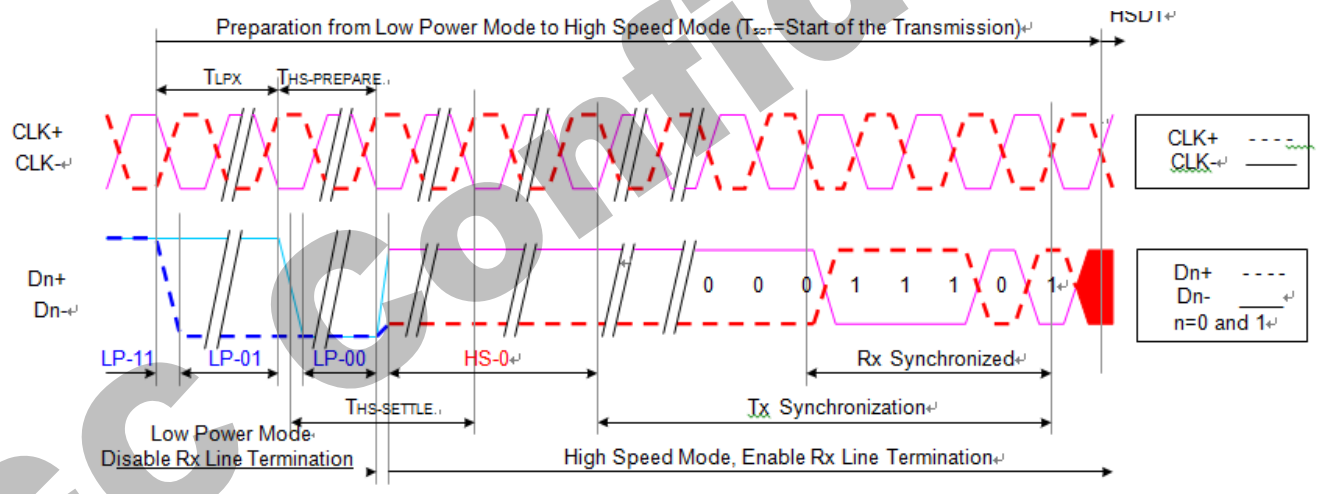


Figure 29 Entering High-Speed Data Transmission (TSOT of HSDT)

5.4.13 Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MPU and this HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

Start: High-Speed Data Transmission (HSDT)

Stops High-Speed Data Transmission

o MPU changes to HS-1, if the last load bit is HS-0 o MPU changes to HS-0, if the last load bit is HS-1

End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

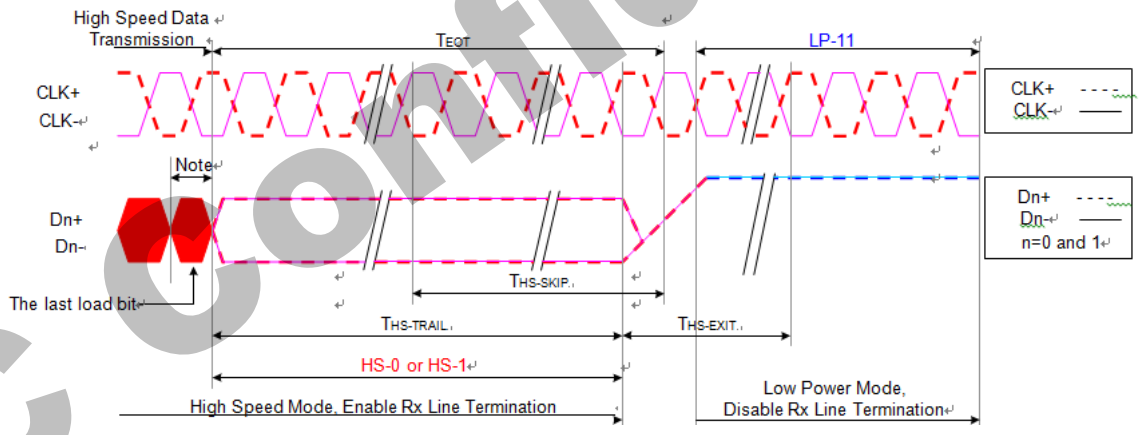


Figure 30 Leaving High-Speed Data Transmission (TEOT of HSDT)Note

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

5.4.14 Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

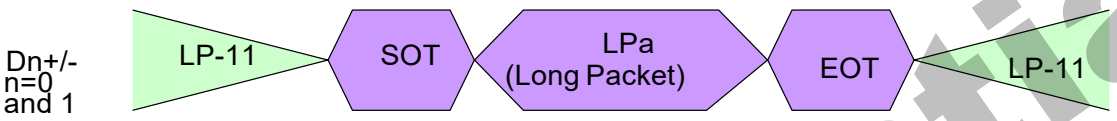
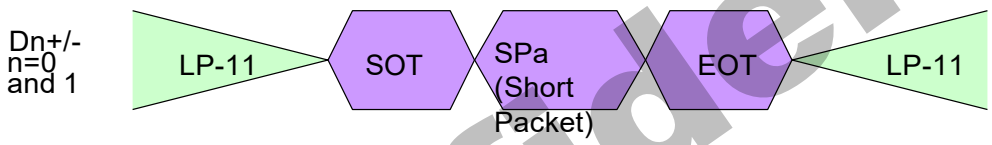


Figure 31 Single Packet in High-Speed Data Transmissions



The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:

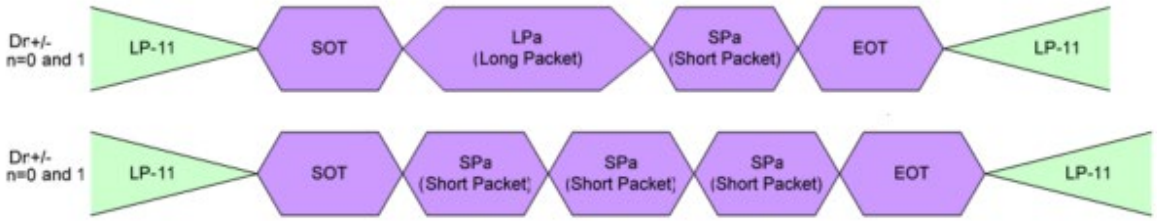


Figure 32 Multiple Packets in High-Speed Data Transmission – Examples

Table 13 Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

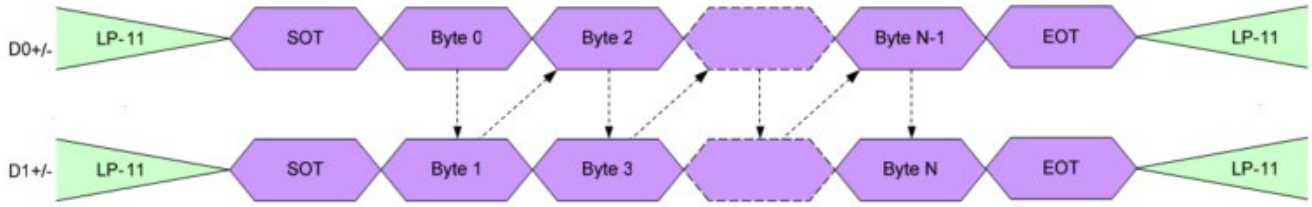


Figure 33 Single Packet in HSDT – Even Number of Bytes

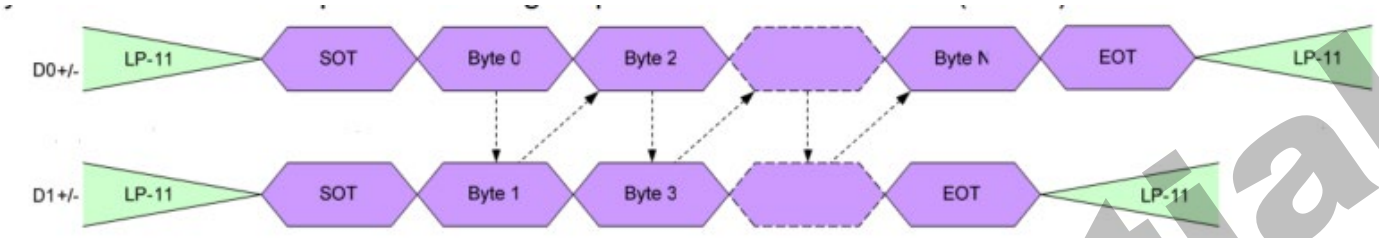


Figure 34 Single Packet in HSDT – Odd Number of Byte

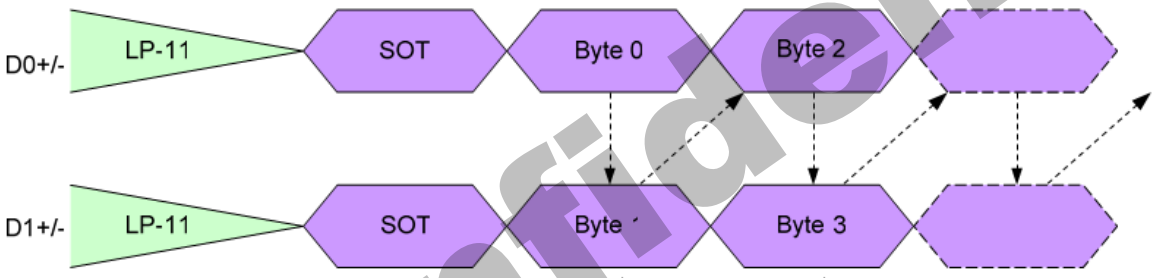


Figure 35 Start of Transmission (SoT) in HSDT for Multiple Packets

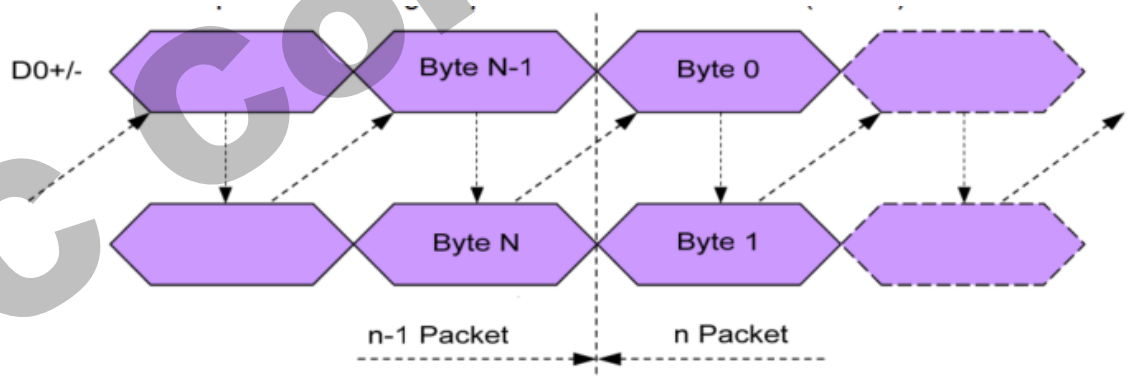


Figure 36 Continue Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

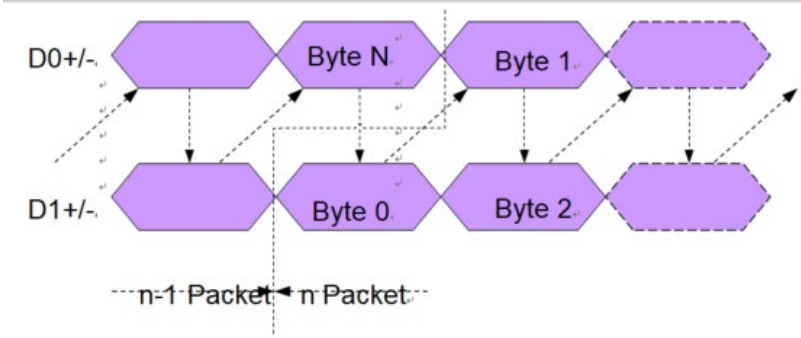


Figure 37 Continue Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

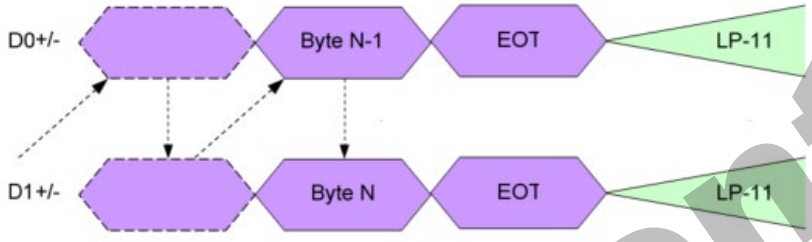


Figure 38 End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

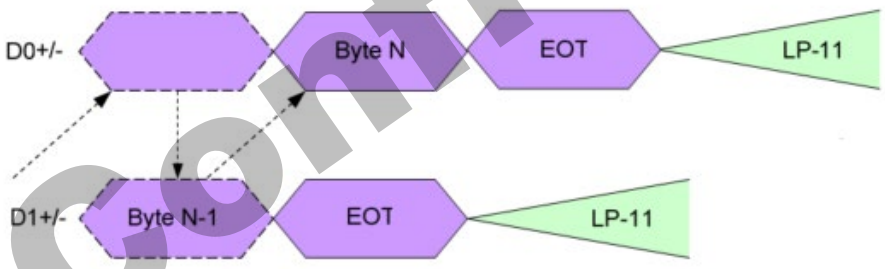


Figure 39 End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at cthe End of the Packet

5.4.15 Bus Turnaround (BTA)

The MPU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MPU or display module.

The MPU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MPU wants to do the bus turnaround procedure to the display module, as follows.

Start (MPU): LP-11

Turnaround Request (MPU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00

The MPU waits until the display module is starting to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)

The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MPU to the display module) is illustrated below

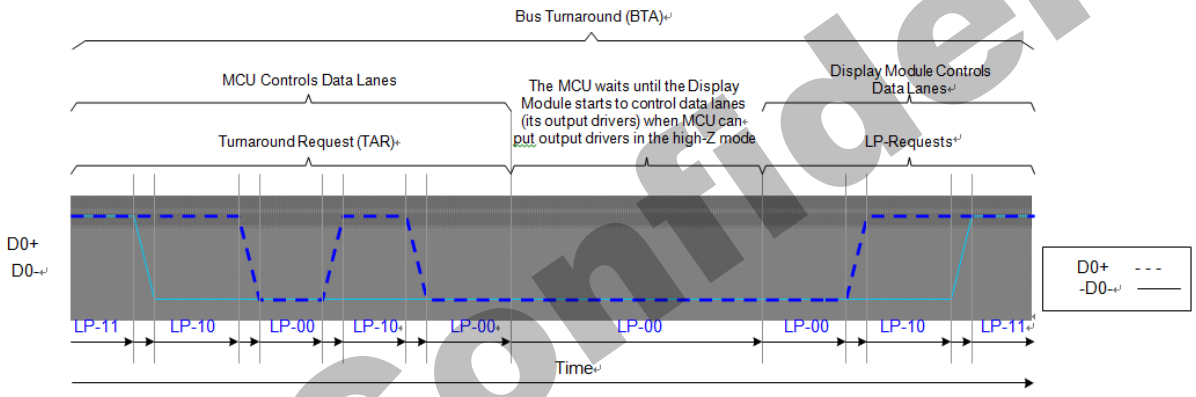


Figure 40 Bus Turnaround Procedure

MPU and display module terms are switched on the Figure 40, if the Bus Turnaround (BTA) is from the display module to the MP

5.4.16 Packet Level Communication

5.4.17 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes[Note].

The lengths of the packets are

Short Packet (SPa): 4 bytes

Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

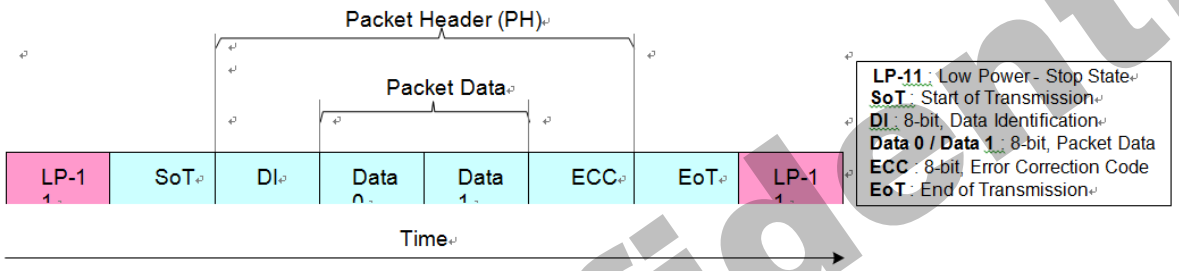


Figure 41 Short Packet (SPa) Structure

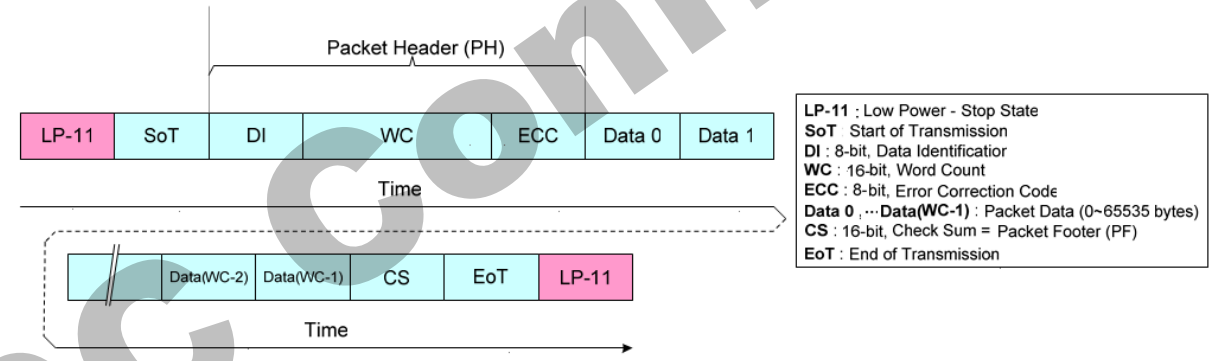


Figure 42 Long Packet (LPa) Structure

Note Short Packet (SPa) and Long Packet (LPa) are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.
LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

5.4.18 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

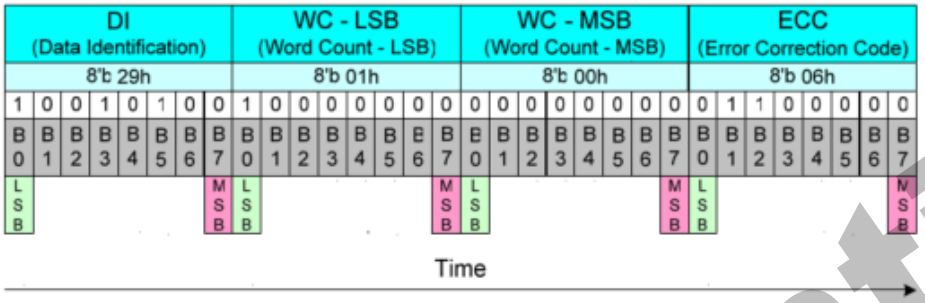


Figure 43 Bit Order of the Byte on Packets

5.4.19 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last

e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

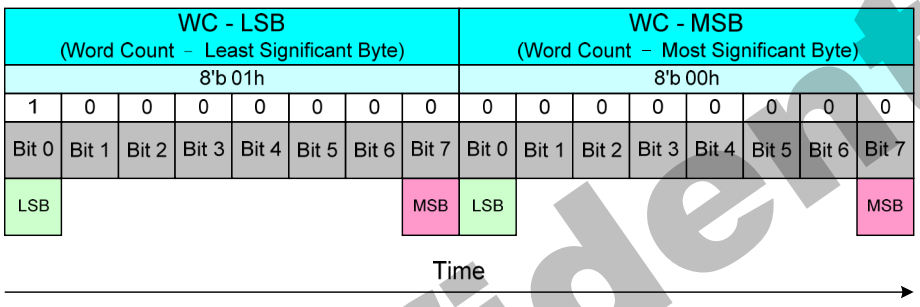


Figure 44 Byte Order of the Multiple Byte Information on Packets

5.4.20 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):
1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

4th byte: Error Correction Code (ECC)

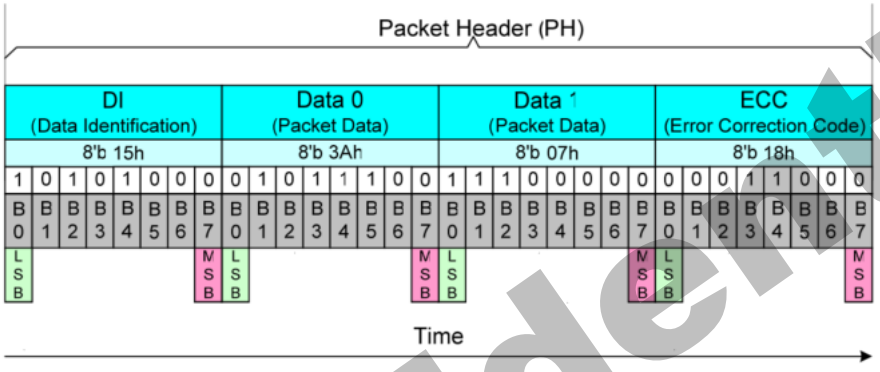


Figure 45 Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):
1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

2nd and 3rd bytes: Word Count (WC)

4th byte: Error Correction Code (ECC)

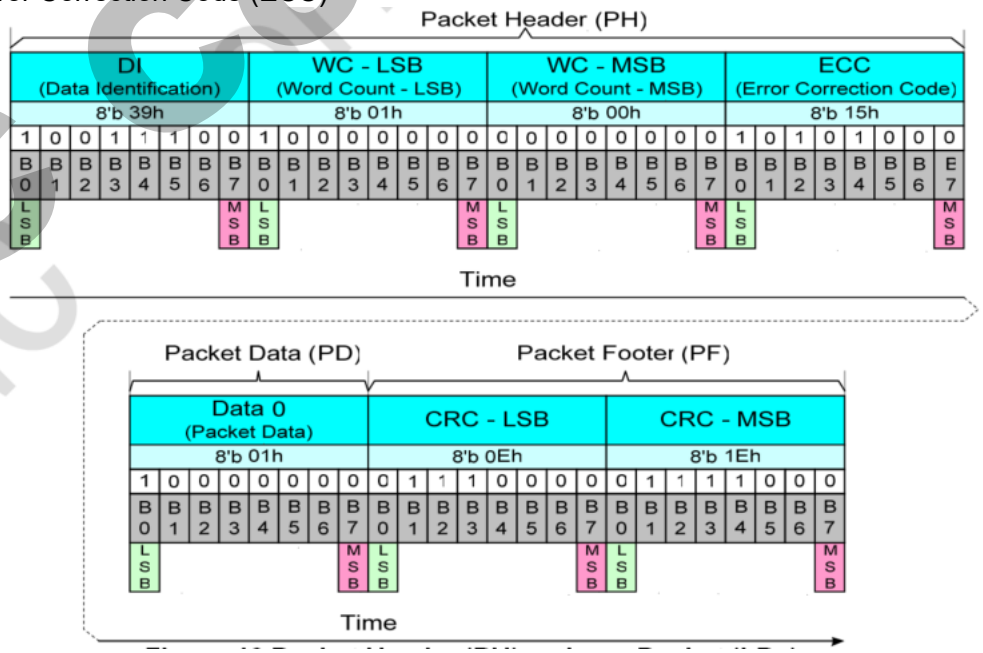


Figure 46 Packet Header (PH) on Long Packet (LPa)

5.4.21 Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

Virtual Channel (VC), 2 bits, DI[7...6]

Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated, see figure below.

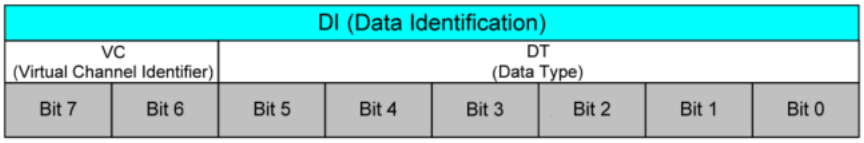


Figure 47 Data Identification (DI) Structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

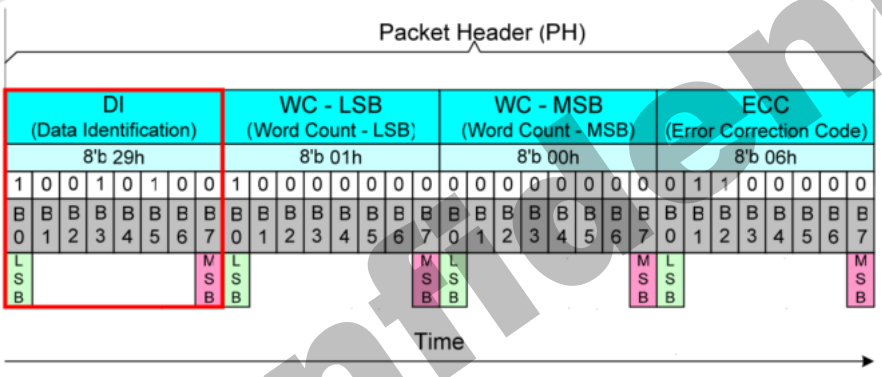


Figure 48 Data Identification (DI) on the Packet Header (PH)

5.4.22 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MPU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

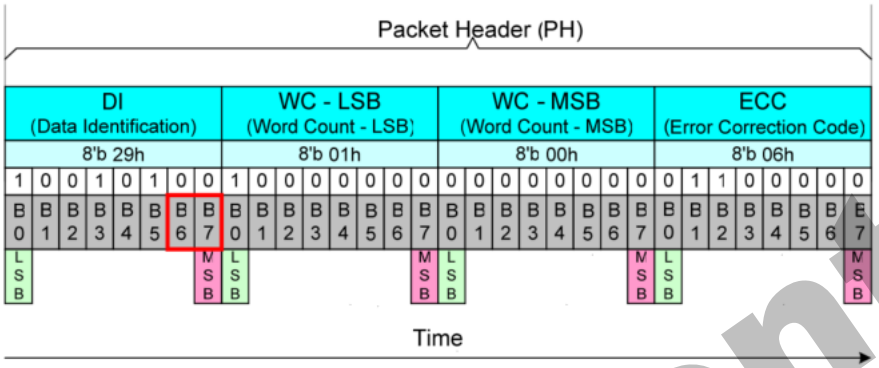


Figure 49 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MPU is using to send packets to them e.g.

The MPU is using the virtual channel 0 when it sends packets to this display module This display module is also using the virtual channel 0 when it sends packets to the MPU This functionality is illustrated below.

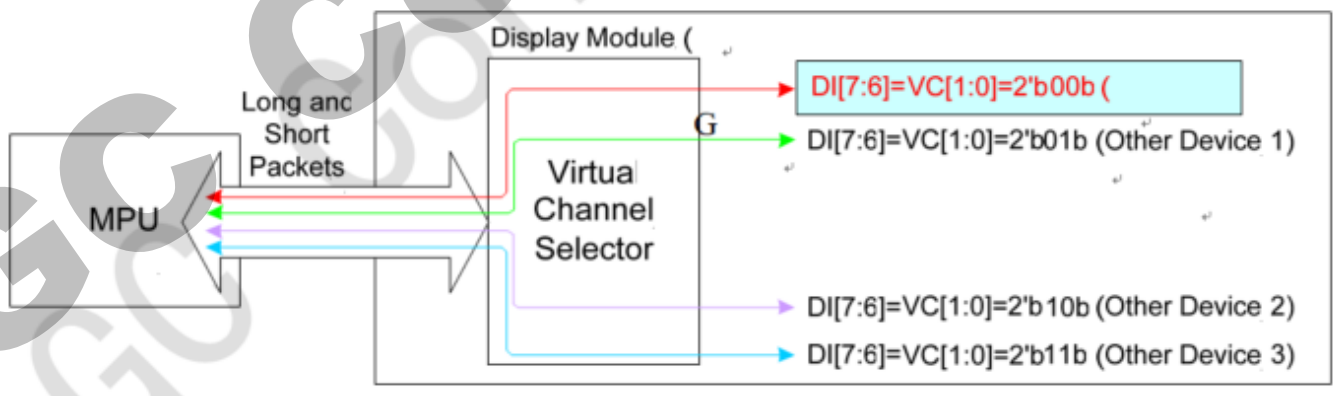


Figure 50 Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00b) when the MPU is sending “End of Transmission Packet” to the display module. See chapter “End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for this display module.

5.4.23 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

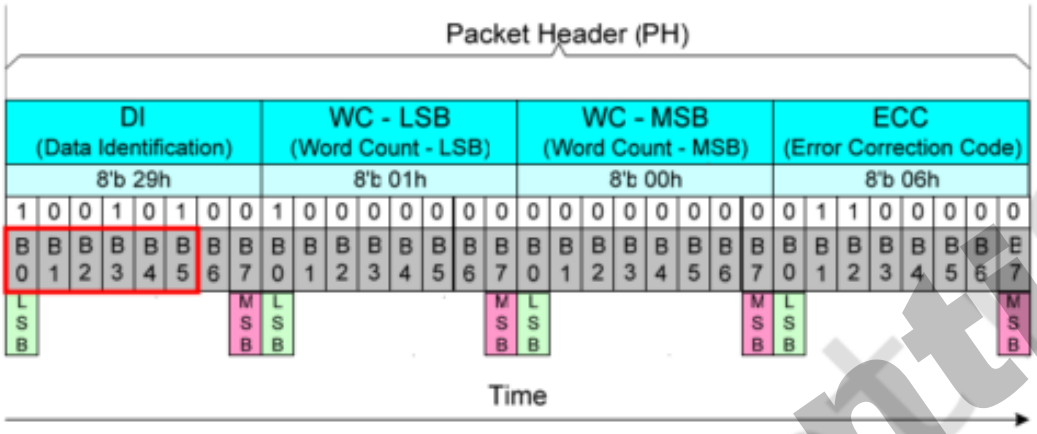


Figure 51 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MPU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

Table 14 Data Type (DT) from the MPU to the Display Module (GC9503NP)

From the MPU to the Display Module (**GC9503NP**)									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note 1	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note 2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Note 1 This can be used when the MPU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

Note 2 This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

Table 15 Data Type (DT) from the Display Module (GC9503NP) to the MPU

From the Display Module (**GC9503NP**) to the MPU									
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver is ignored other Data Type (DT) if they are not defined on tables: “ Table 14 Data Type (DT) from the MPU to the Display Module (or Other Devices)” or “ Table 15 Data Type (DT) from the Display Module (or Other Devices) to the MPU”.

5.4.24 Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

Data 1: 01hex (DCS's parameter)

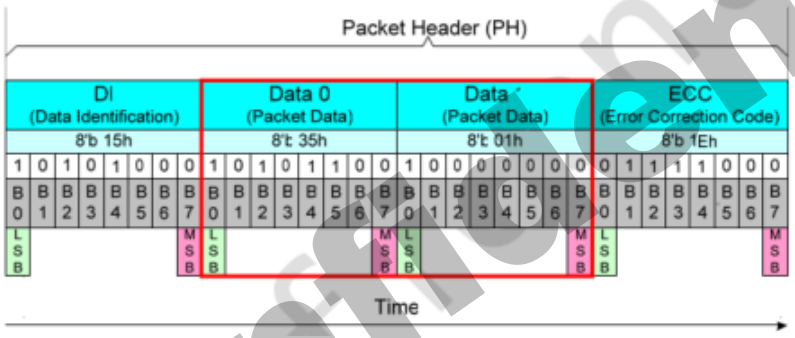


Figure 52 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

Data 1: 00hex (Null)

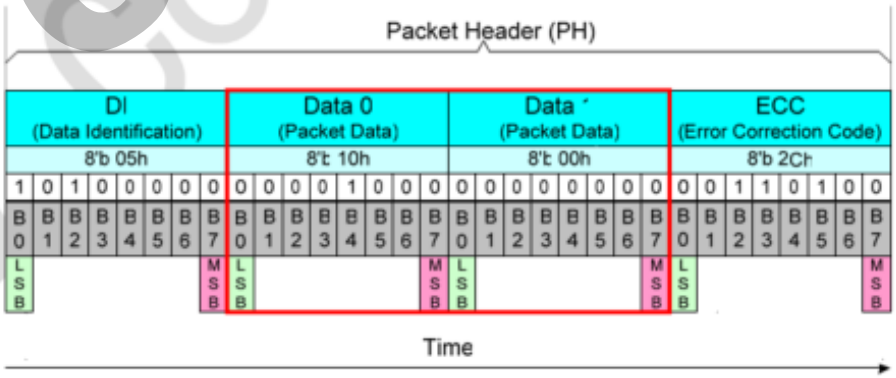


Figure 53 Packet Data (PD) for Short Packet (SPa), 1 Byte Information

5.4.25 Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

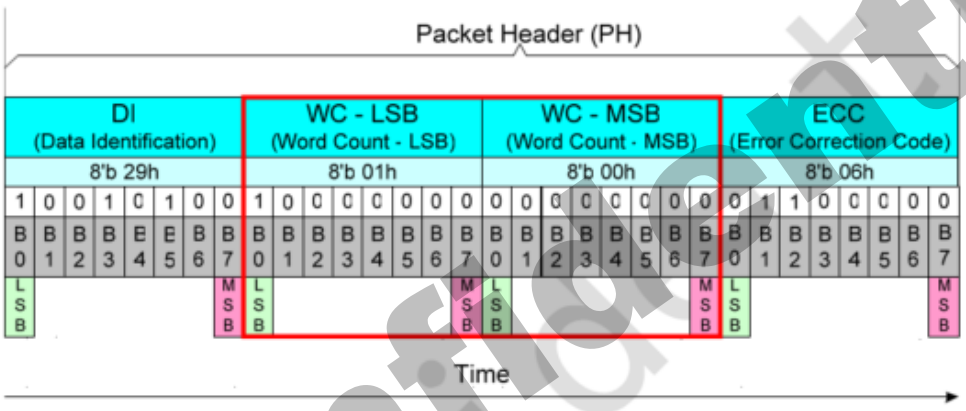


Figure 54 Word Count (WC) on the Long Packet (LPa)

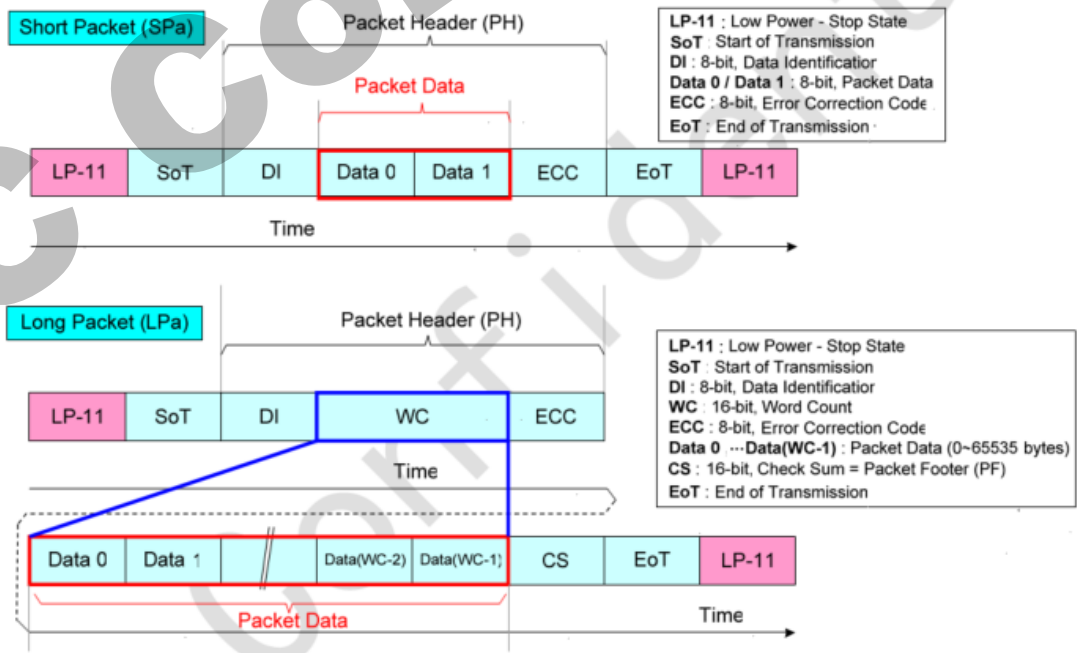


Figure 55 Packet Data in Short and Long Packets

5.4.26 Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0…7]), Packet Data (PD) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

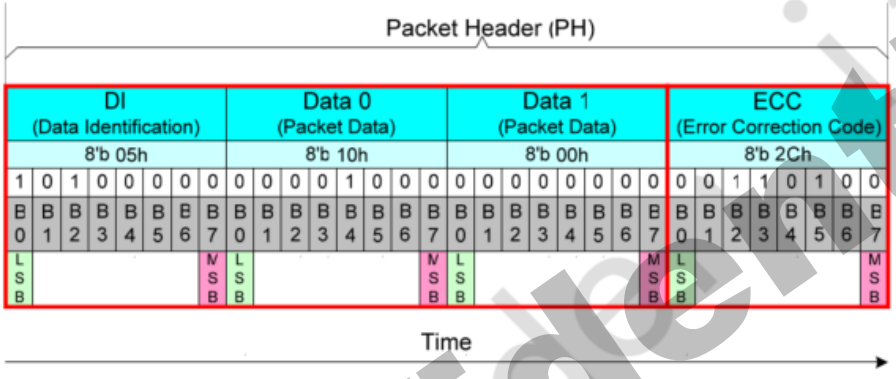


Figure 56 D[23…0] and P[7…0] on the Short Packet (SPa)

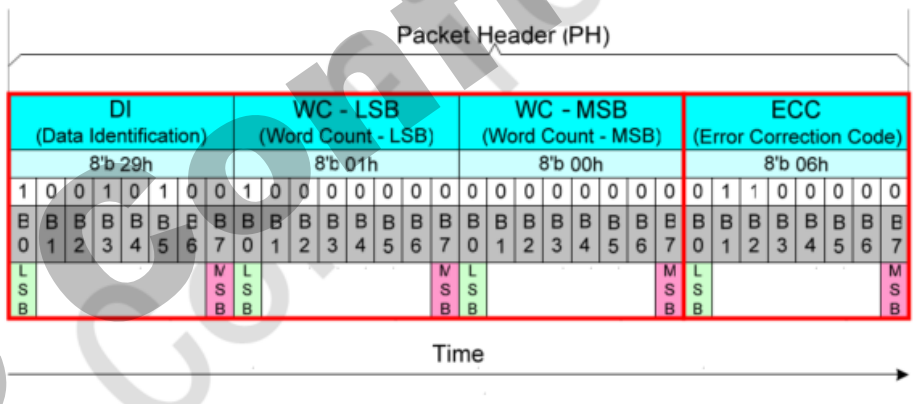


Figure 57 D[23…0] and P[7…0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

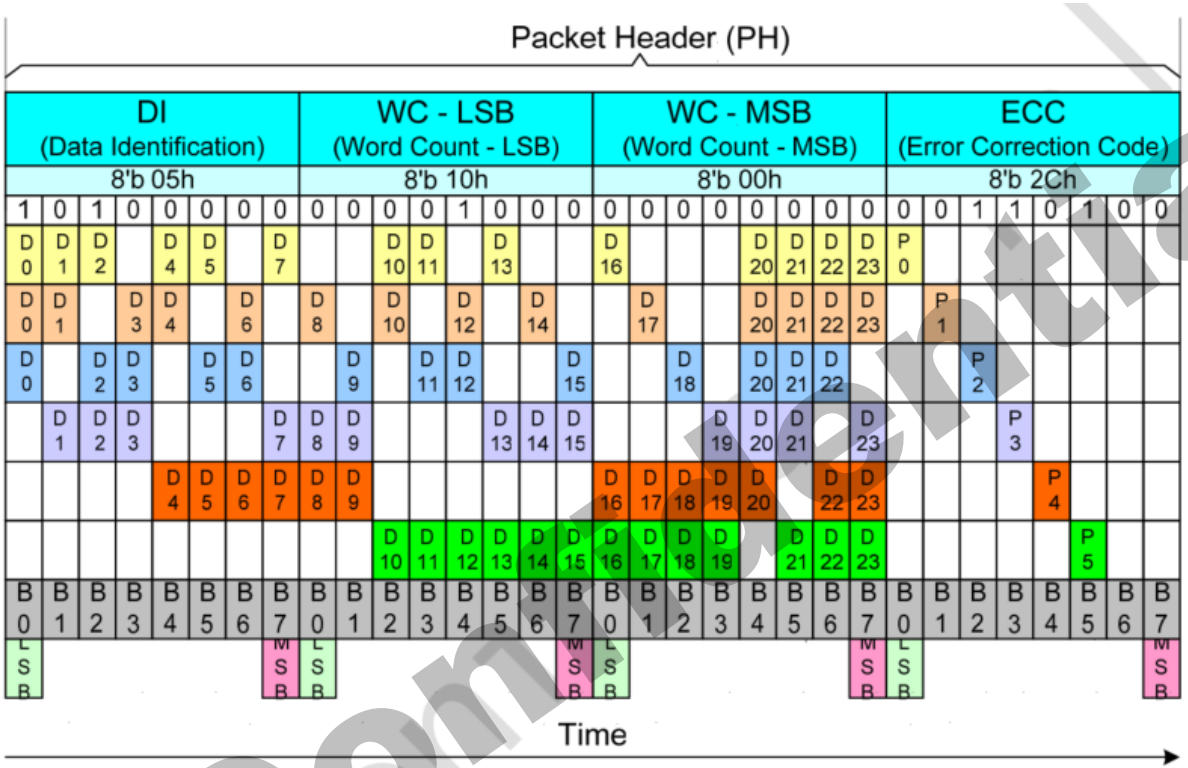


Figure 58 XOR Functionality on the Short Packet (SPa)

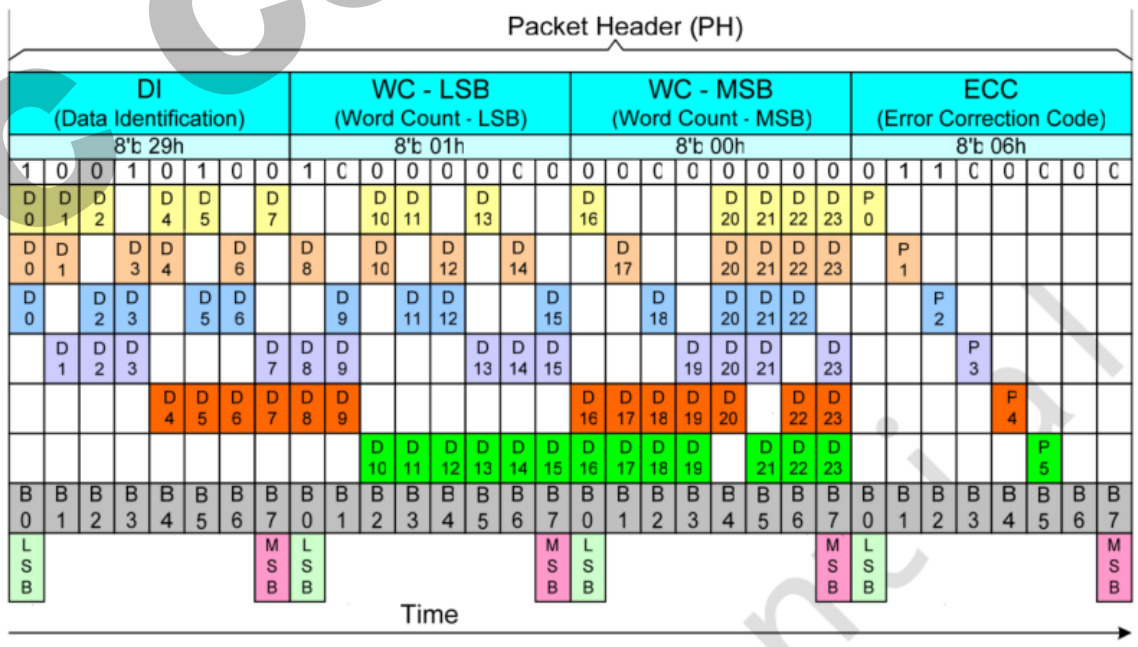


Figure 59 XOR Functionality on the Long Packet (LPa)

The transmitter (The MPU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MPU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MPU and the receiver is the display module, is illustrated for reference purposes below.

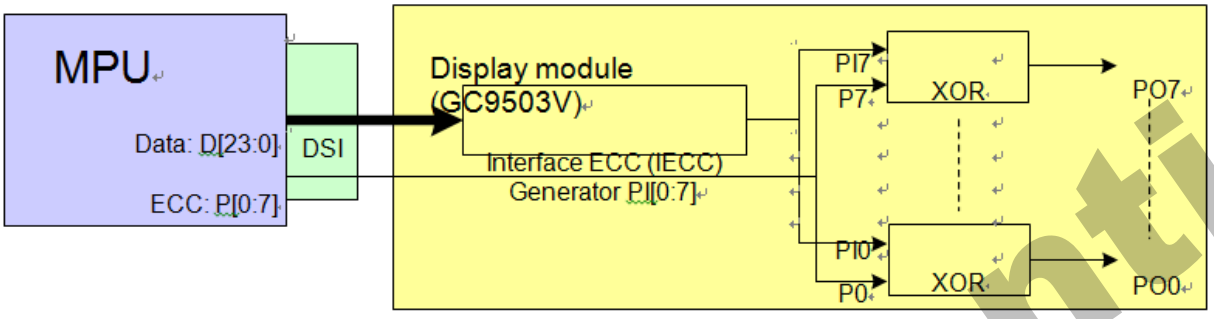


Figure 60 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h. The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 61 Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 62 Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Table 16 One Bit Error Value of the Error Correction Code (ECC)

Data	P	P	P	P	P	P	P	P	H
D[0]	0	0	0	0	0	1	1	1	07
D[1]	0	0	0	0	1	0	1	1	0B
D[2]	0	0	0	0	1	1	0	1	0
D[3]	0	0	0	0	1	1	1	0	0E

D[4]	0	0	0	1	0	0	1	1	13
D[5]	0	0	0	1	0	1	0	1	15
D[6]	0	0	0	1	0	1	1	0	16
D[7]	0	0	0	1	1	0	0	1	19
D[8]	0	0	0	1	1	0	1	0	1A
D[9]	0	0	0	1	1	1	0	0	1
D[10]	0	0	1	0	0	0	1	1	23
D[11]	0	0	1	0	0	1	0	1	25
D[12]	0	0	1	0	0	1	1	0	26
D[13]	0	0	1	0	1	0	0	1	29
D[14]	0	0	1	0	1	0	1	0	2A
D[15]	0	0	1	0	1	1	0	0	2
D[16]	0	0	1	1	0	0	0	1	31
D[17]	0	0	1	1	0	0	1	0	32
D[18]	0	0	1	1	0	1	0	0	34
D[19]	0	0	1	1	1	0	0	0	38
D[20]	0	0	0	1	1	1	1	1	1F
D[21]	0	0	1	0	1	1	1	1	2F
D[22]	0	0	1	1	0	1	1	1	37
D[23]	0	0	1	1	1	0	1	1	3B

One error is detected if the value of the PO[7…0] is on Table 25: One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on Table 25: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

5.4.27 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

5.4.28 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa). The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

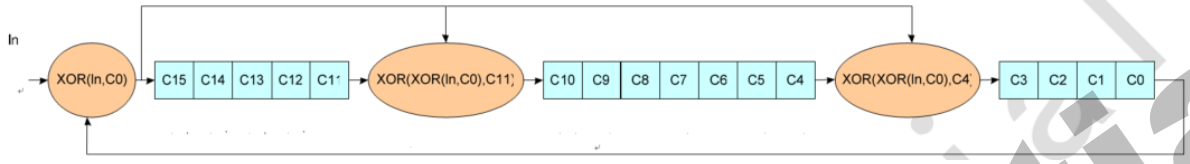
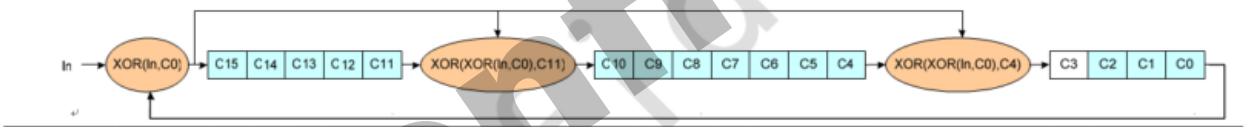


Figure 63 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.
The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).
An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	↑	↑	1	1	↑	X	↑	↑	↑	1	1	1	↑	X	↑	1	↑	↑	X
↑	1(LSB)	0	0	↑	1	1	↑	↑	↑	↑	↑	1	1	1	↑	↑	↑	1	↑	↑	↑
2	0	↑	↑	0	1	1	↑	0	0	↑	↑	1	1	1	↑	0	0	1	↑	↑	↑
3	0	↑	↑	↑	0	1	↑	0	0	0	↑	1	1	1	↑	0	0	0	↑	↑	↑
4	0	↑	↑	↑	1	0	↑	0	0	0	0	1	1	1	↑	0	0	0	0	↑	↑
5	0	↑	↑	↑	1	1	0	0	0	0	0	0	1	1	↑	0	0	0	0	0	0
6	0	0	0	↑	1	1	↑	0	0	0	0	0	0	1	↑	↑	↑	0	0	0	0
7	0	0	0	0	1	1	↑	↑	↑	0	0	0	0	0	↑	↑	↑	1	0	0	0
8	0(MSB)	0	0	0	0	1	↑	↑	↑	↑	0	0	0	0	0	↑	↑	1	↑	0	0
	1 byte	CRC result	0	0	0	1	↑		↑	↑	0	0	0	0	0		↑	1	↑	0	
			MSB																	LSB	

Figure 64 CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

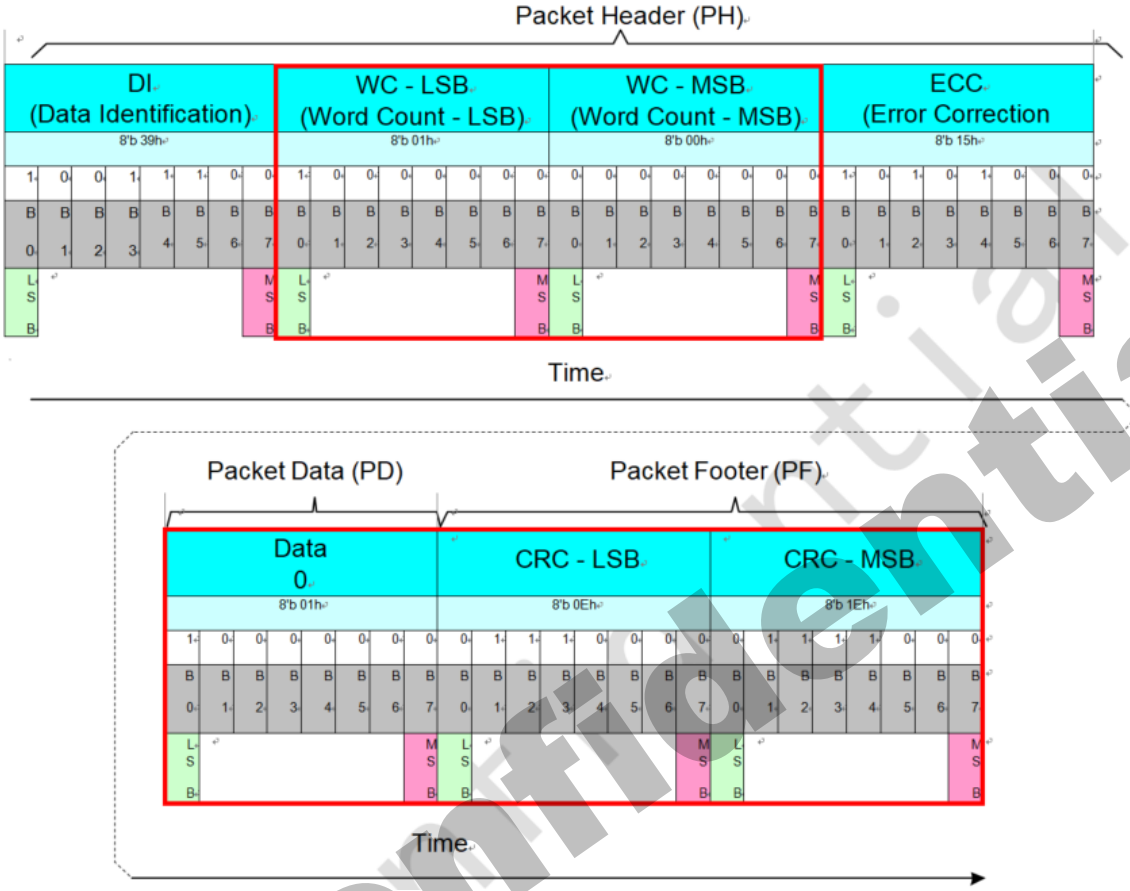


Figure 65 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.4.29 Packet Transmissions

5.4.29.1 Packet from the MPU to the Display Module

5.4.29.1.1 Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “5.2. Command Description” is used from the MPU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

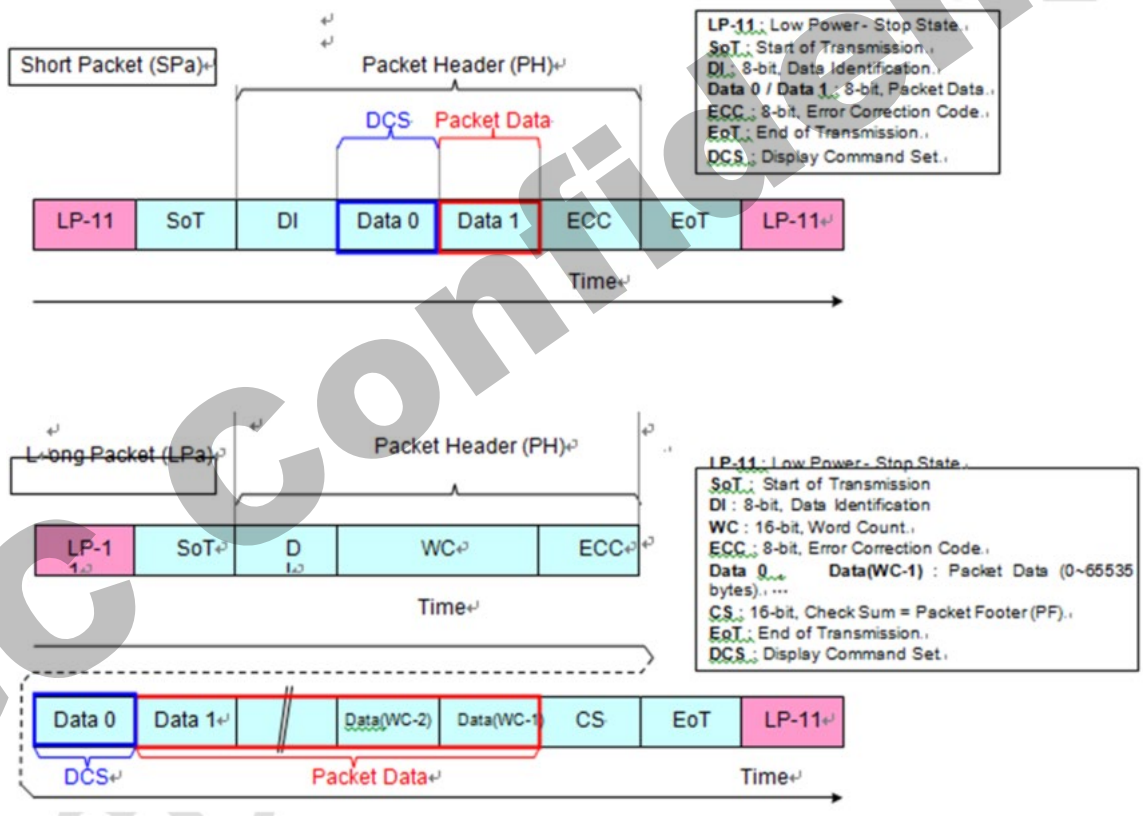


Figure 66 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

5.4.29.1.1.1 Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MPU to the display module. These commands are defined on a table below. (See chapter "Command Description")

Table 17 Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Page 0 Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 00

0101b

Packet Data (PD)

o Data 0: "Sleep In (10h)", Display Command Set

(DCS) o Data 1: Always 00hex

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

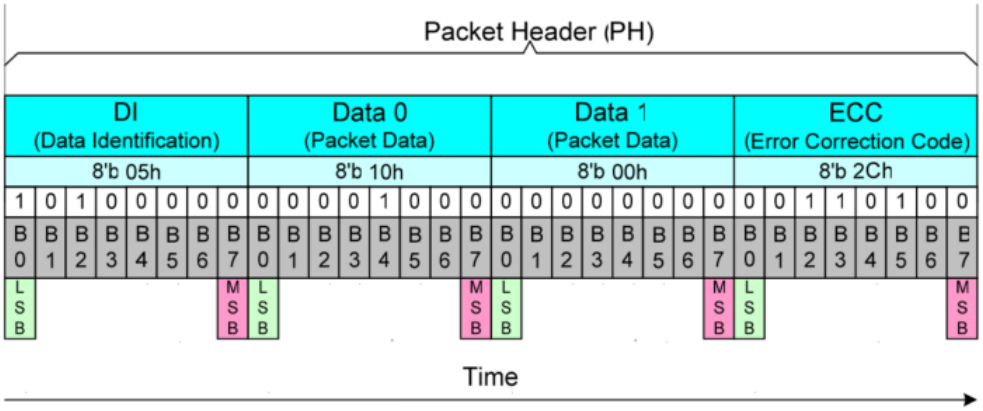


Figure 67 Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

5.4.29.1.1.2 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MPU to the display module. These commands are defined on a table (See chapter "Command Description") below.

Table 18 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Page 0 Command
Gamma Set (26h)
Interface Pixel Format (3Ah)
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness
Write CABC Minimum Brightness

Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 01

0101b

Packet Data (PD)

o Data 0: "Gamma Set (26h)", Display Command Set

(DCS) o Data 1: 01hex, Parameter of the DCS

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

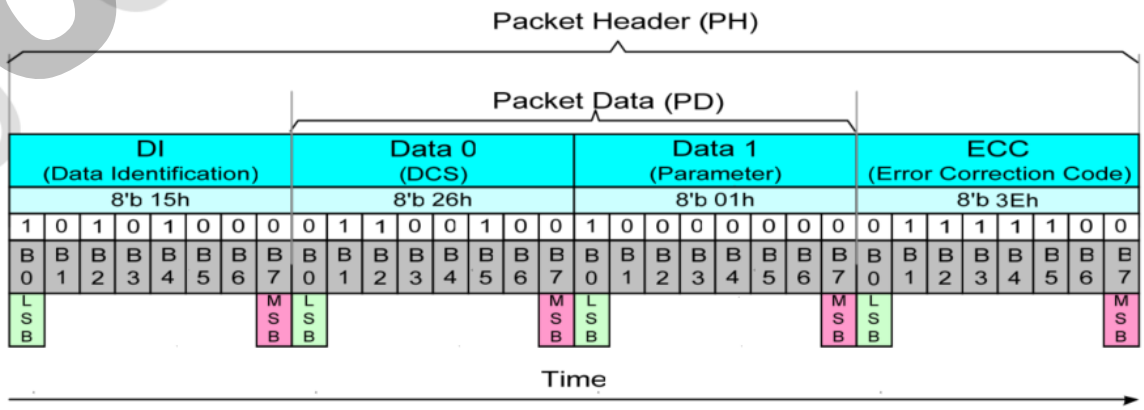


Figure 68 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

5.4.29.1.1.3 Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MPU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "Command Description") below.

Table 19 Display Command Set (DCS) Write Long (DCSW-L)

Page 0 Command
NOP (00h)
Software Reset (01h),Note1
Sleep In(10h) ,Note1
Sleep Out (11h) ,Note1
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Gamma Set (26h) ,Note2
Display Off (28h) ,Note1
Display ON (29h) ,Note1
Interface Pixel Format (3Ah)
Write Display Brightness (51h) ,Note2
Write CTRL Display (53h) ,Note2
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Note 1 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, No Parameter"

Note 2 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, 1 Parameter"

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 11

1001b

Word Count (WC)

o Word Count (WC): 0001h

Error Correction Code (ECC)

Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

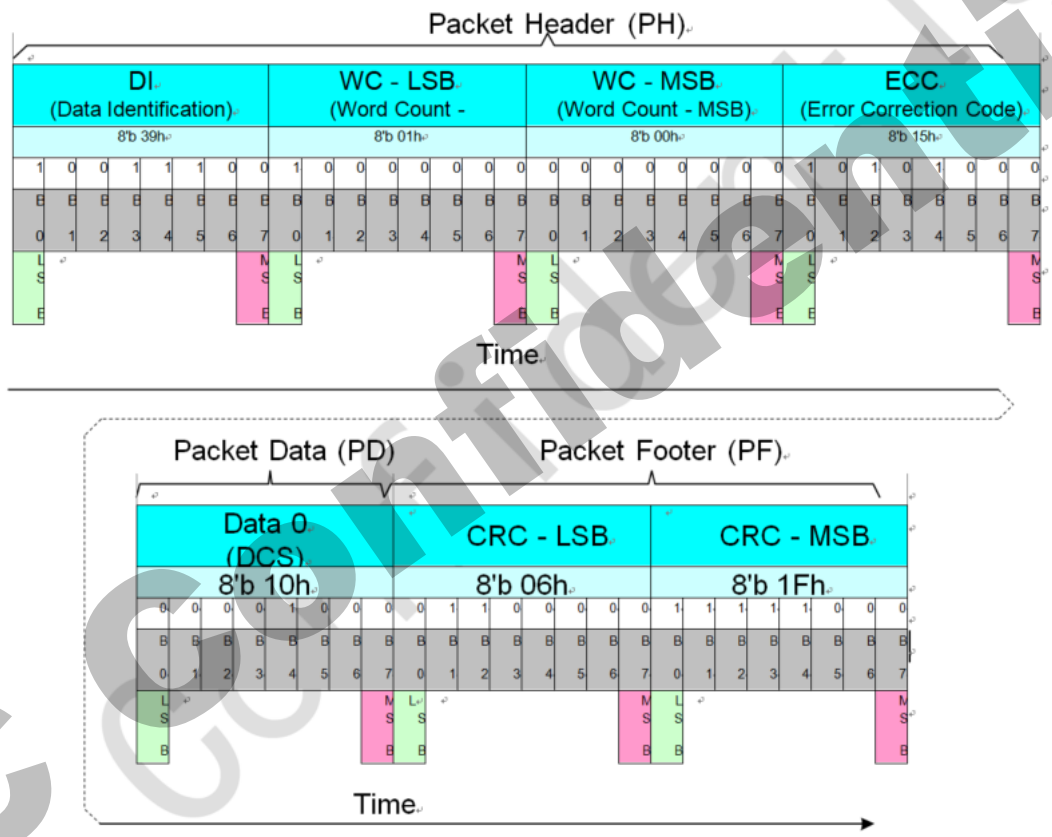


Figure 69 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 11

1001b

Word Count (WC)

o Word Count (WC): 0002h

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: “Gamma Set (26h)”, Display Command Set

(DCS) o Data 1: 01hex, Parameter of the DCS

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

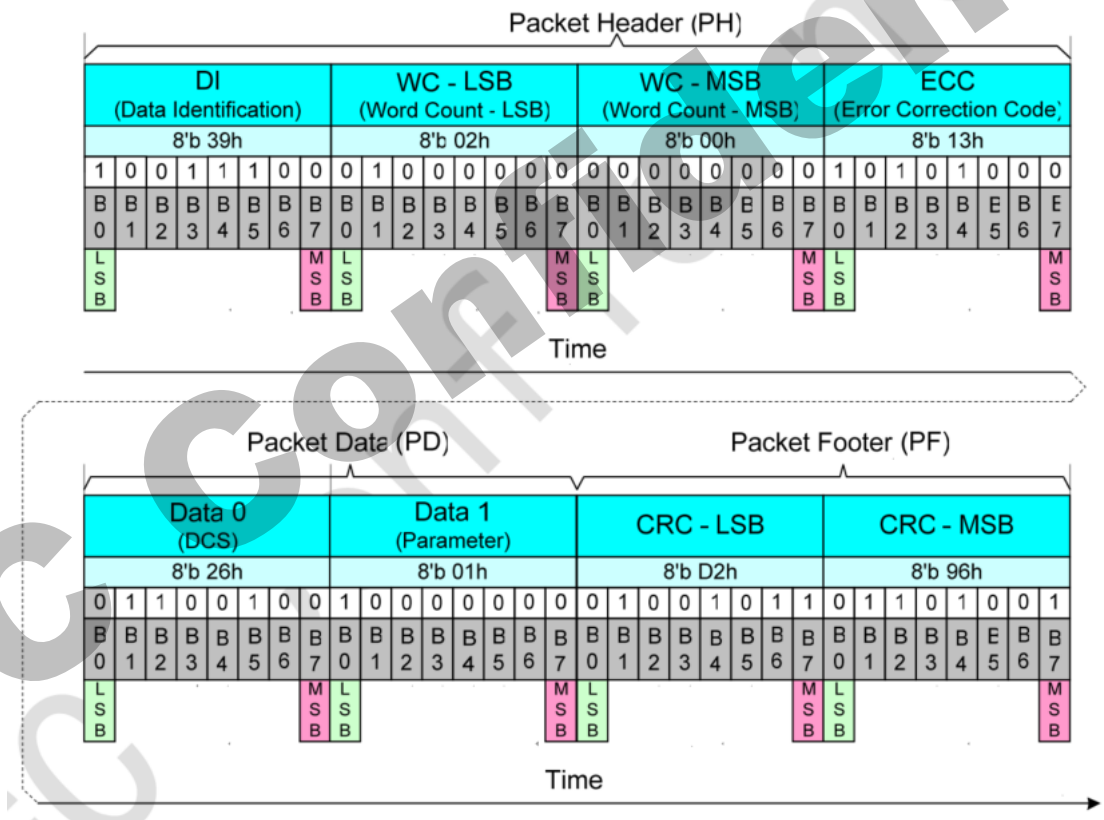


Figure 70 Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 11

1001b

Word Count (WC)

o Word Count (WC): 0005h

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: “Column Address Set (2Ah)”, Display Command Set

(DCS) o Data 1: 00hex, 1st Parameter of the DCS, Start Column

SC[15…8] o Data 2: 12hex, 2nd Parameter of the DCS, Start

Column SC[7…0] o Data 3: 01hex, 3rd Parameter of the DCS,

End Column EC[15…8] o Data 4: EFhex, 4th Parameter of the

DCS, End Column EC[7…0]

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

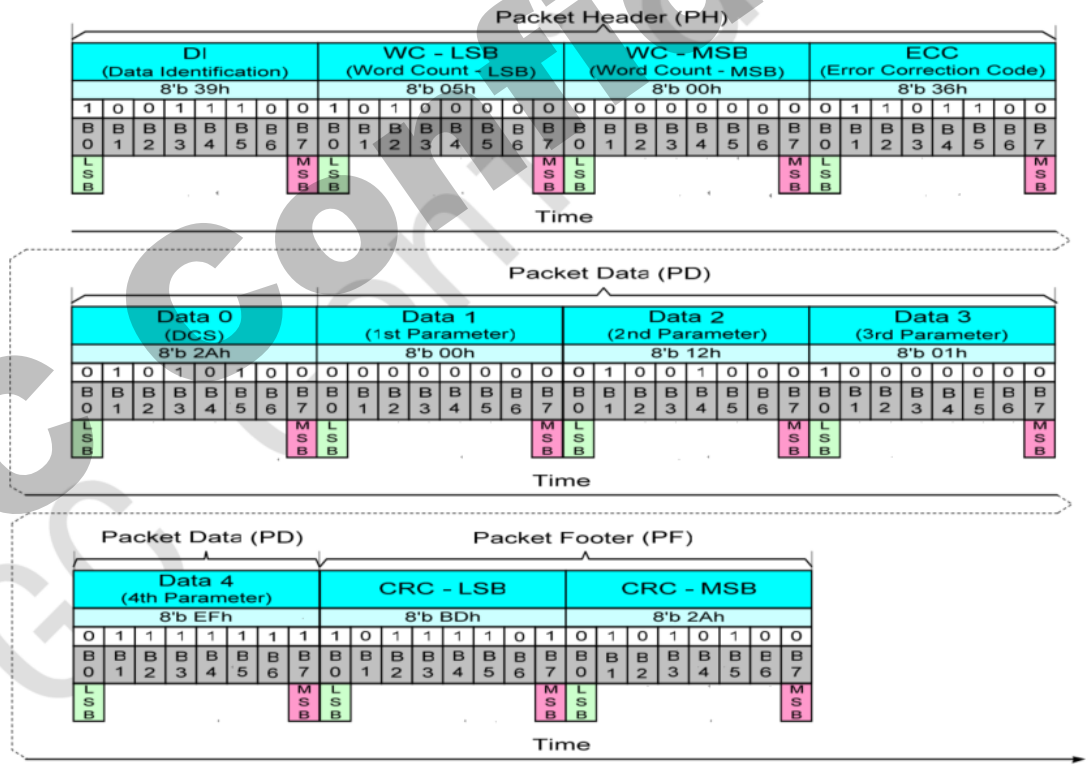


Figure 71 Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

5.4.29.1.1.4 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MPU to the display module. These commands are defined on a table (See chapter "5.2. Command Description") below.

Table 20 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Page 0 Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control
Read CABC Minimum Brightness (5Fh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MPU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MPU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

The MPU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 11

0111b

Maximum Return Packet Size (MRPS) o

Data 0: 01hex

o Data 1: 00hex

Error Correction Code (ECC)

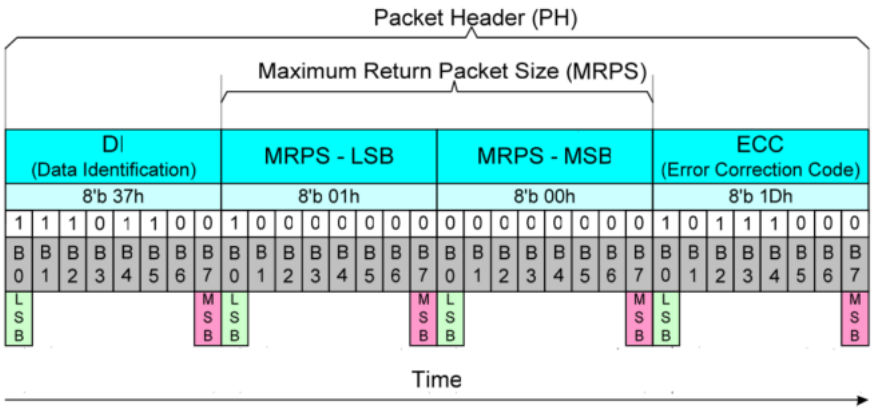


Figure 72 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MPU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MPU sends “Display Command Set (DCS) Read, No Parameter” to the display module

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 00

0110b

Packet Data (PD)

o Data 0: “Read ID1 (DAh)”, Display Command Set

(DCS) o Data 1: Always 00hex

Error Correction Code (ECC)

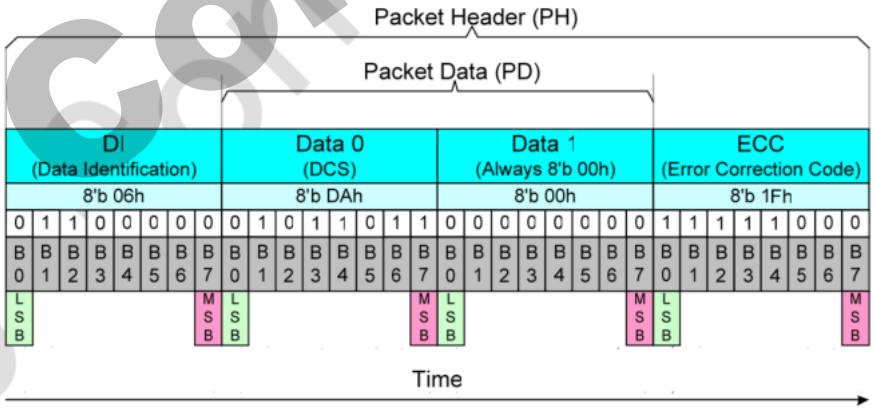


Figure 73 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MPU after Bus Turnaround (BTA)

An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command, See chapter “Acknowledge with Error Report (AwER)”

Information of the received command. Short Packet (SPa) or Long Packet (LPa)

5.4.29.1.1.5 Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MPU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed.

The display module is ignored Packet Data (PD) what the MPU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 00

1001b

Word Count (WC)

o Word Count (WC): 0005hex

Error Correction Code (ECC)

Packet Data (PD):

o Data 0: 89hex (Random data) o Data 1: 23hex (Random data) o Data 2: 12hex (Random data) o Data 3: A2hex (Random data) o Data 4: E2hex (Random data)

Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

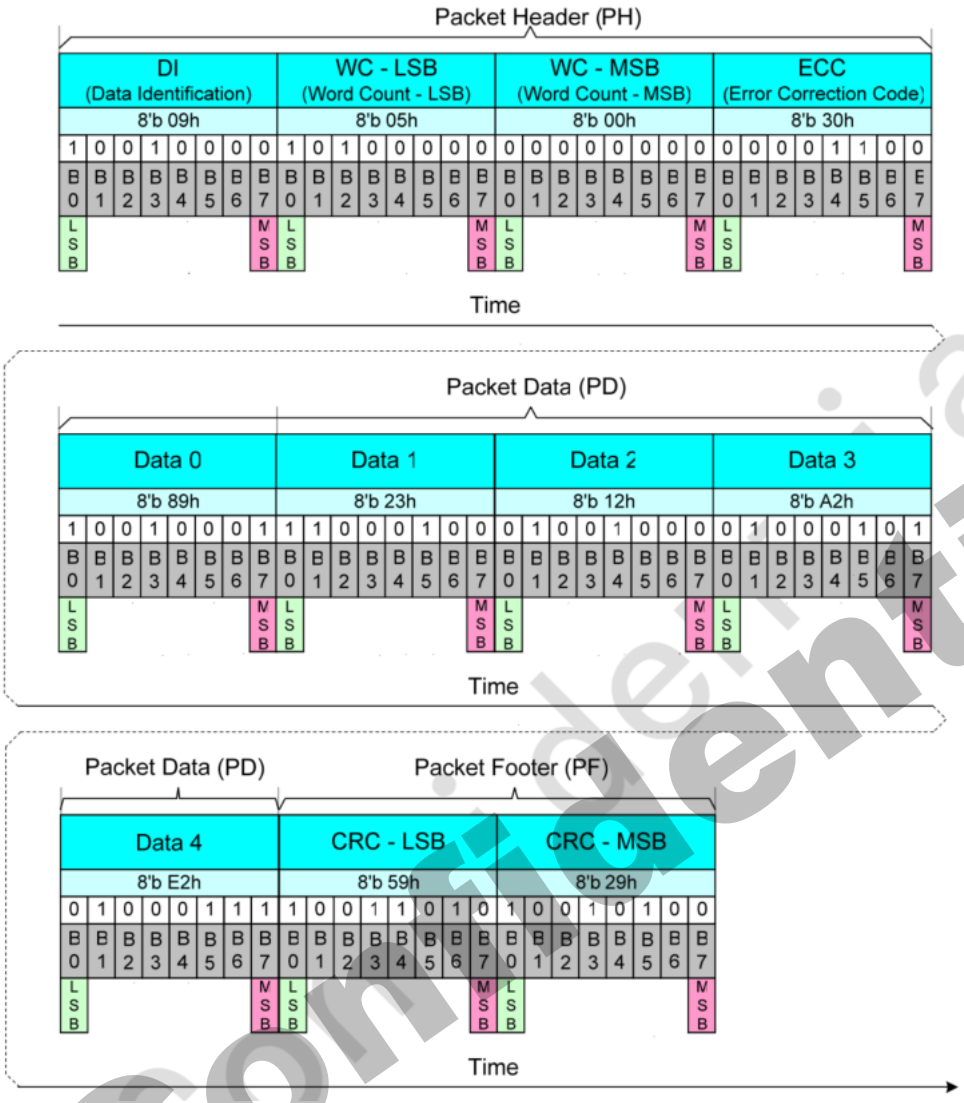


Figure 74 Null Packet, No Data (NP-L) - Example

End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MPU to the display module. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MPU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both: i.e. If the MPU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MPU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MPU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 21 Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MPU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MPU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) is using a fixed format as follows
Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 00

1000b

Packet Data (PD)

o Data 0: 0Fhex

o Data 1: 0Fhex

Error Correction Code (ECC) o

ECC: 01hex

This is defined on the Short Packet (SPa) as follows.

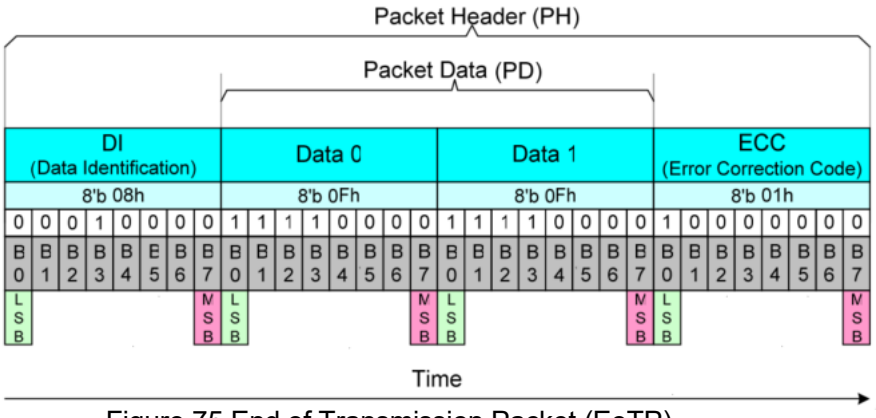


Figure 75 End of Transmission Packet (EoTP)

Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.

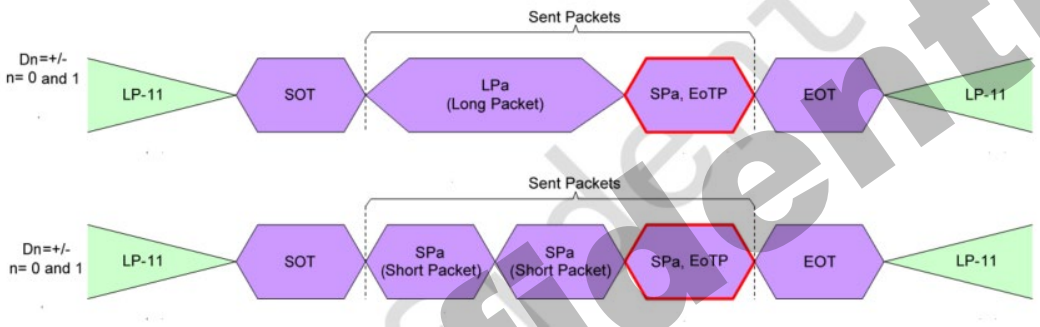


Figure 76 End of Transmission Packet (EoTP)-Examples

5.4.29.2 Packet from the Display Module to the MPU

5.4.29.2.1 Used Packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MPU after the MPU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “Data Type (DT)”. It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

Both cases are illustrated for reference purposes below.

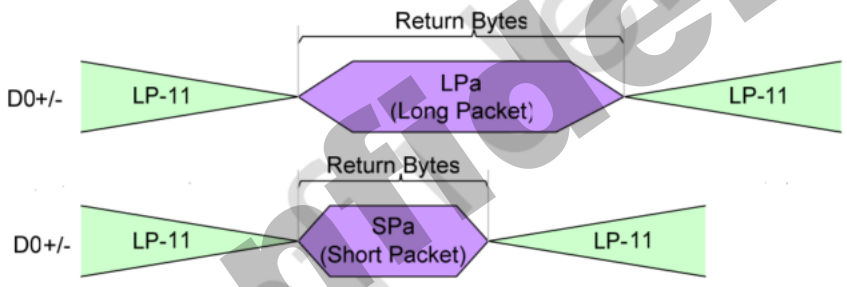


Figure 77 Return Bytes on Single Packet

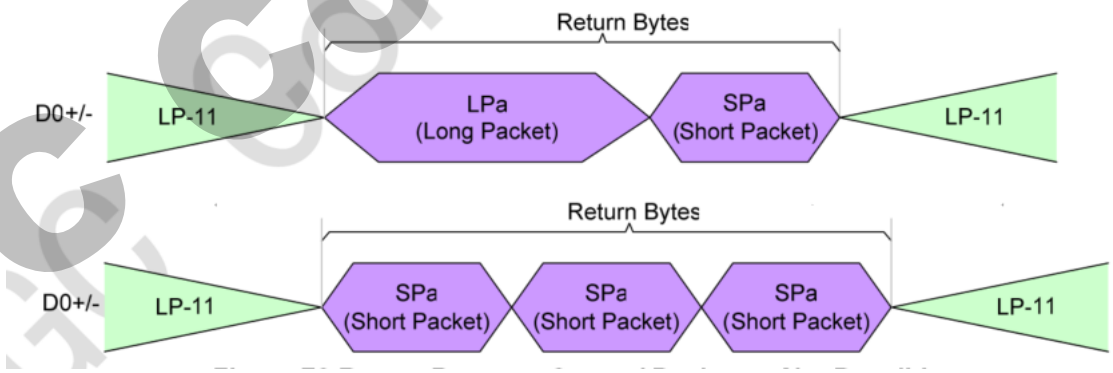


Figure 78 Return Bytes on Several Packets – Not Possible

Exception:

The display module is returning 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MPU when the display module has received a read command (See chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) where has been detected and corrected a single bit error by the EEC (See bit 8 on “Table 22: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”).

These return packets are illustrated for reference purposes below.

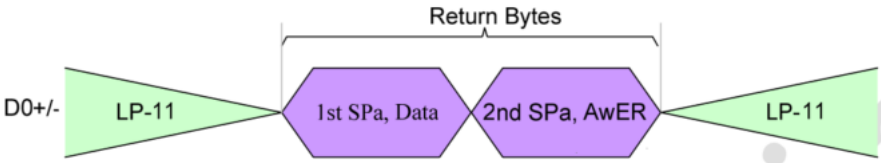


Figure 79 Exception when Return Bytes on Several Packets

AwER = Acknowledge with Error Report

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MPU. The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Table 22 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

B	Description
0	SoT Error
1	SoT Sync
2	EoT Sync
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 23 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

B	Description
0	SoT Error
1	SoT Sync
2	EoT Sync
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to '0' internally Set to '0' internally (Only for Long Packet
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

These errors are included from all packages what has been received from the MPU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

Data Identification (DI)

o Virtual Channel (VC, DI[7…6]):

00b o Data Type (DT, DI[5…0]): 00

0010b

Packet Data (PD)

o Bit 8: ECC Error, single-bit (detected and

corrected) o AwER: 0100h

Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

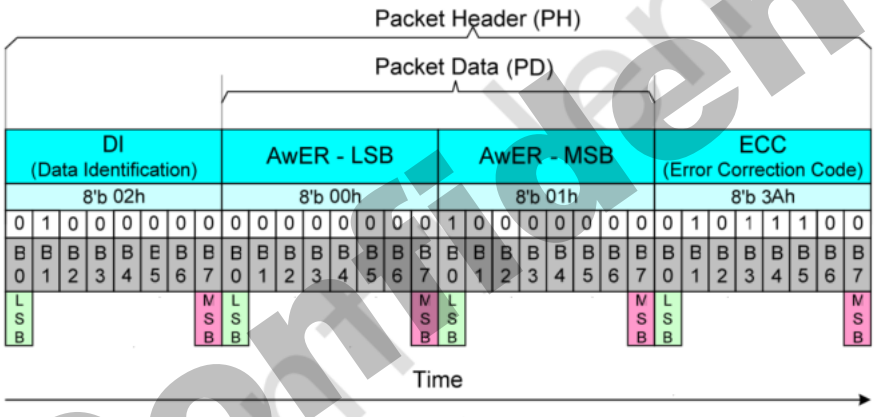


Figure 80 Acknowledge with Error Report (AwER) – Example

It is possible that the display module has received several packets, which have included errors, from the MPU before the MPU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

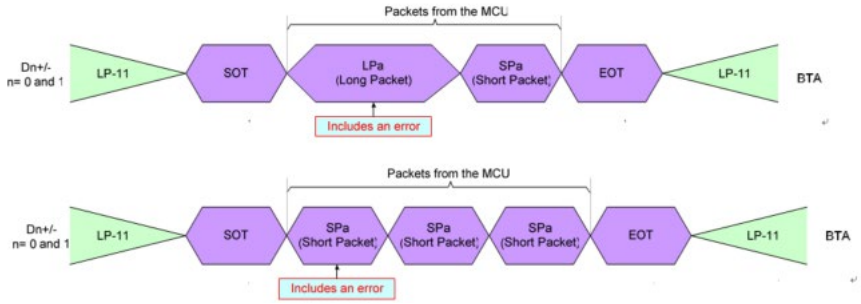


Figure 81 Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ***ECC or CRC*** error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MPU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.

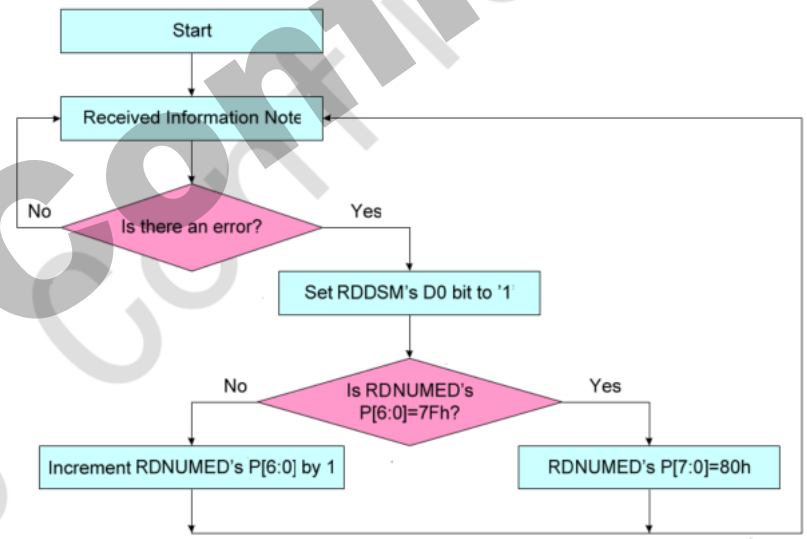


Figure 82 Flow Chart for Errors on DSI[Note]

Note 1. This information can be Interface or Packet Level Communication but it is always from the MPU to the display module in this case.

2. CRC or ECC error

5.4.29.2.2 DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 011100b), from the display module to the MPU.“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module. Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD)

Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

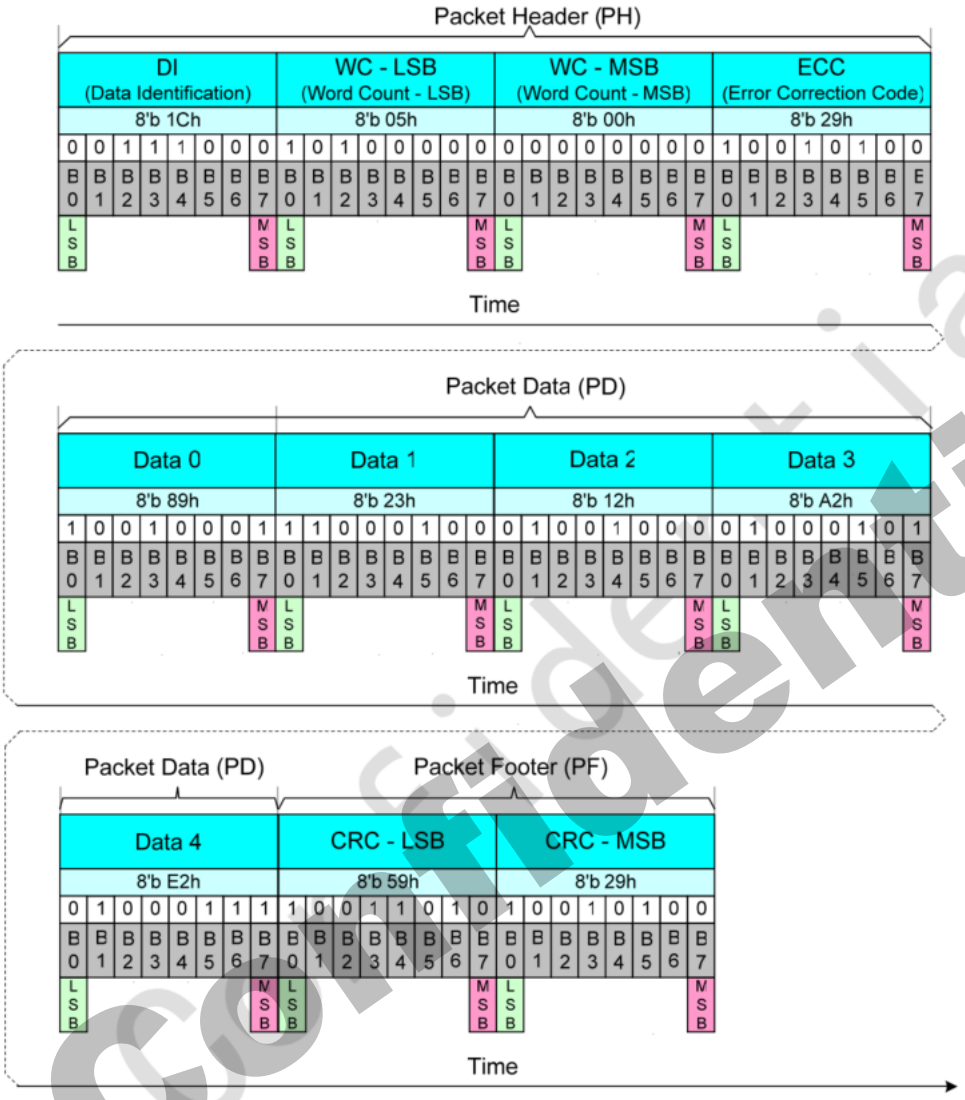


Figure 83 DCS Read Long Response (DCSRR-L) - Example

5.4.29.2.3 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MPU.“DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

Data Identification (DI)

Virtual Channel (VC, DI[7…6]):

00b

Data Type

(DT, DI[5…0]): 10 0001b

Packet Data

(PD) Data 0:

45hex

Data 1: 00hex (Always)

Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

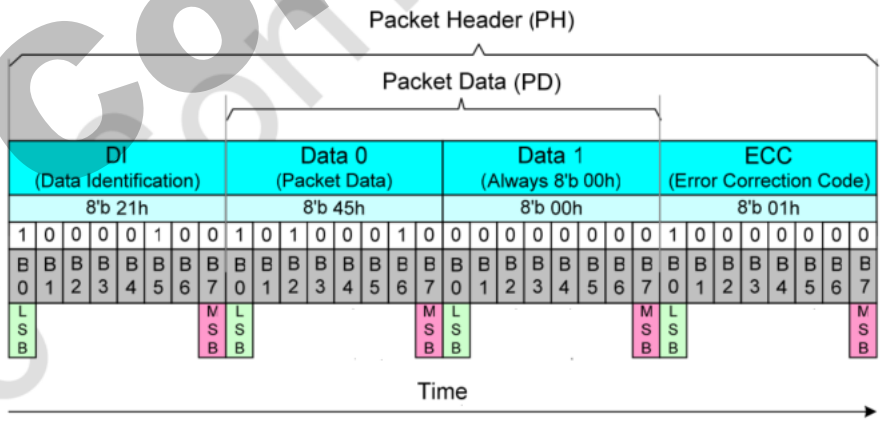


Figure 84 DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

5.4.29.2.4 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MPU."DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.
Short Packet (SPa) is defined e.g.

This is defined on the Short Packet (SPa) as follows.

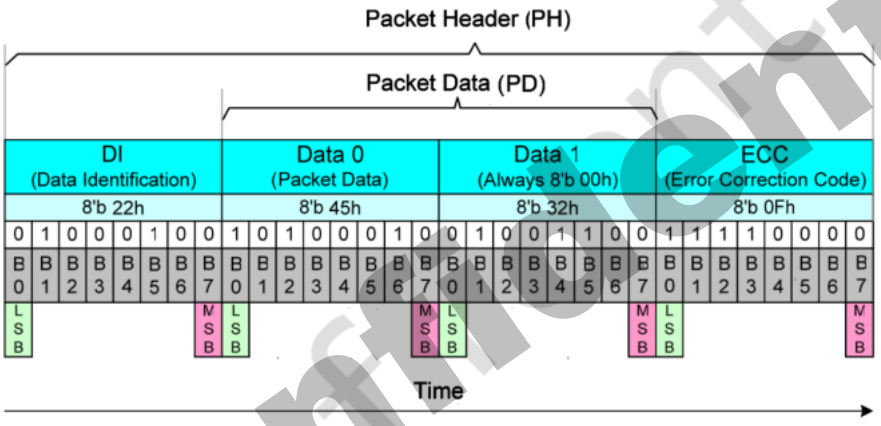


Figure 85 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

5.4.30 Communication Sequences

The communication sequences can be done on interface or packet levels between the MPU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.
This communication sequence description is for DSI data lanes (DSI-D0+/- and DSI-D1+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See chapter “DSI-CLK Lanes”.
Functions of the interface level communication is described on the following table.

Table 24 Interface Level Communication

Interface	Abbreviati	Interface Action
Low Power	LP-11	Stop State
	LPDT	Low Power Data
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High	HSDT	High speed Data

Functions of the packet level communication are described on the following table.

Table 25 Packet Level Communication

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MPU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
Display Module (GC9503V)	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

5.4.30.1 DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

Table 26 DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	- -	LP-11	- +	- -	--	Start
2	DCSW 1-S	LPDT	- +	- -	-	
3	- -	LP-11	- +	- -	--	End

Table 27 DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	- +	--	- -	Start
2	DCSW1-S	HSDT	- +	--	- -	
3	EoTP	HSDT	- +	--	--	End of Transmission Packet
4	--	LP-11	- +	--	- -	End

5.4.30.2 DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

Table 29 DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	- -	LP-11	- +	- -	- -	Start
2	DCSWN-S	LPDT	-+	--	--	
3	- -	LP-11	- +	- -	- -	End

Table 30 DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	- +	- -	- -	Start
2	DCSWN-S	HSDT	- +	- -	- -	
3	EoTP	HSDT	- +	--	--	End of Transmission Packet
4	- -	LP-11	- +	- -	- -	End

5.4.30.3 DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 32 DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	- -	LP-11	-+	- -	- -	Start
2	DCSW-L	LPDT	-+	- -	- -	
3	- -	LP-11	-+	- -	- -	End

Table 33 DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	-+	-	-	Start
2	DCSRN-S	HSDT	-+	- -	- -	
3	EoTP	HSDT	-+	- -	--	End of Transmission Packet
4	-	LP-11	-+	-	-	End

5.4.30.4 DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

5.4.30.5 Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Null Packet, No Data Sequence - Example						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	-+	- -	--	Start
2	NP-L	HSDT	-+	- -	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	-+	- -	--	End of Transmission Packet
4	--	LP-11	-+	- -	--	End

Table 37 Null Packet, No Data Sequence - Example

5.4.30.6 End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined on chapter “8.1.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

Table 38 End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MPU		Information Direction	Display Module (**GC9503NP**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	-+	- -	--	Start
2	NP-L	HSDT	-+	- -	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	-+	- -	--	End of Transmission Packet
4	--	LP-11	-+	- -	--	End

5.5 Display Data Format

5.5.1 DPI (RGB) Interface

5.5.1.1 16-bit / pixel 65K colors order on the DPI Interface

The 16-bit RGB interface is selected by setting the DPI[2:0] bits to “101”. The display operation is synchronized with VS, HS and PCLK signals.

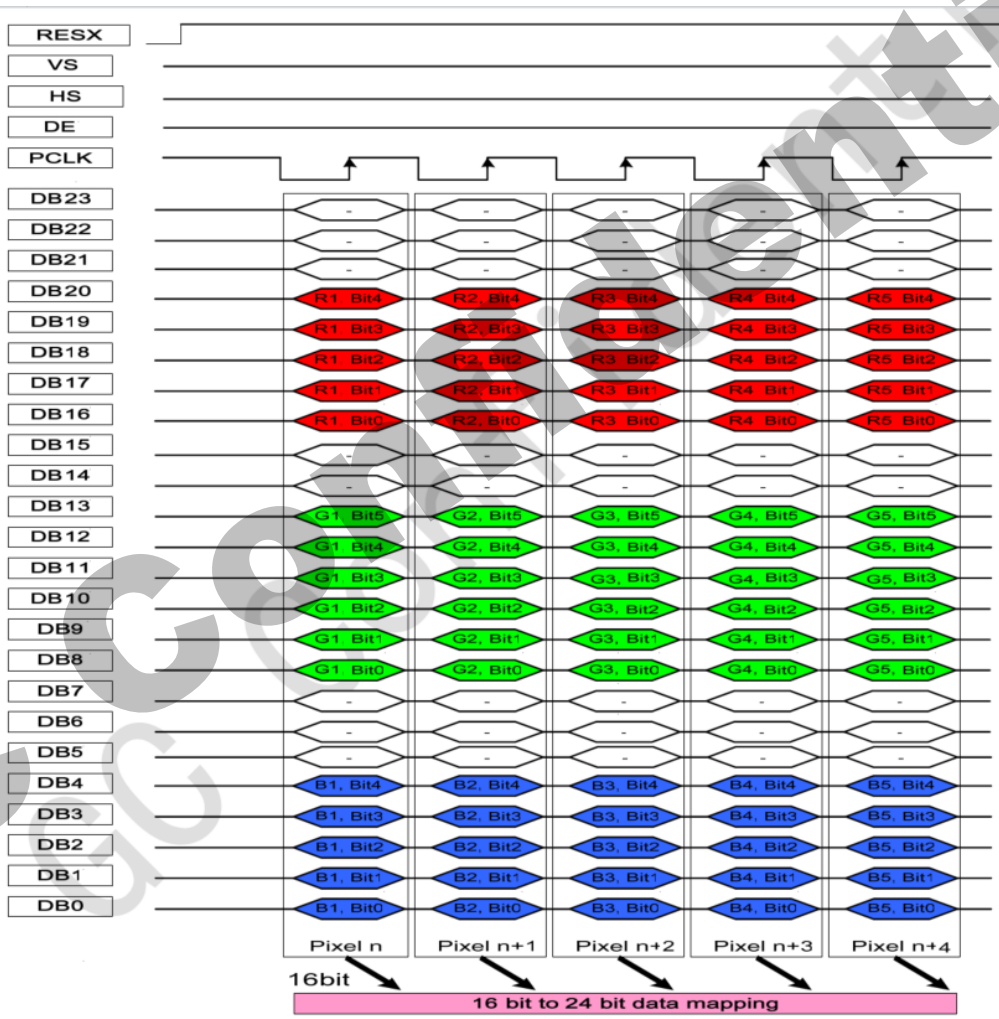


Figure 86 16-bit / pixel 65K colors order on the DPI Interface

Note:

The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

1-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.

‘-‘= void

5.5.1.2 18-bit / pixel 262K colors order on the DPI Interface

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to “110”. The display operation is synchronized with VS, HS and PCLK signals.

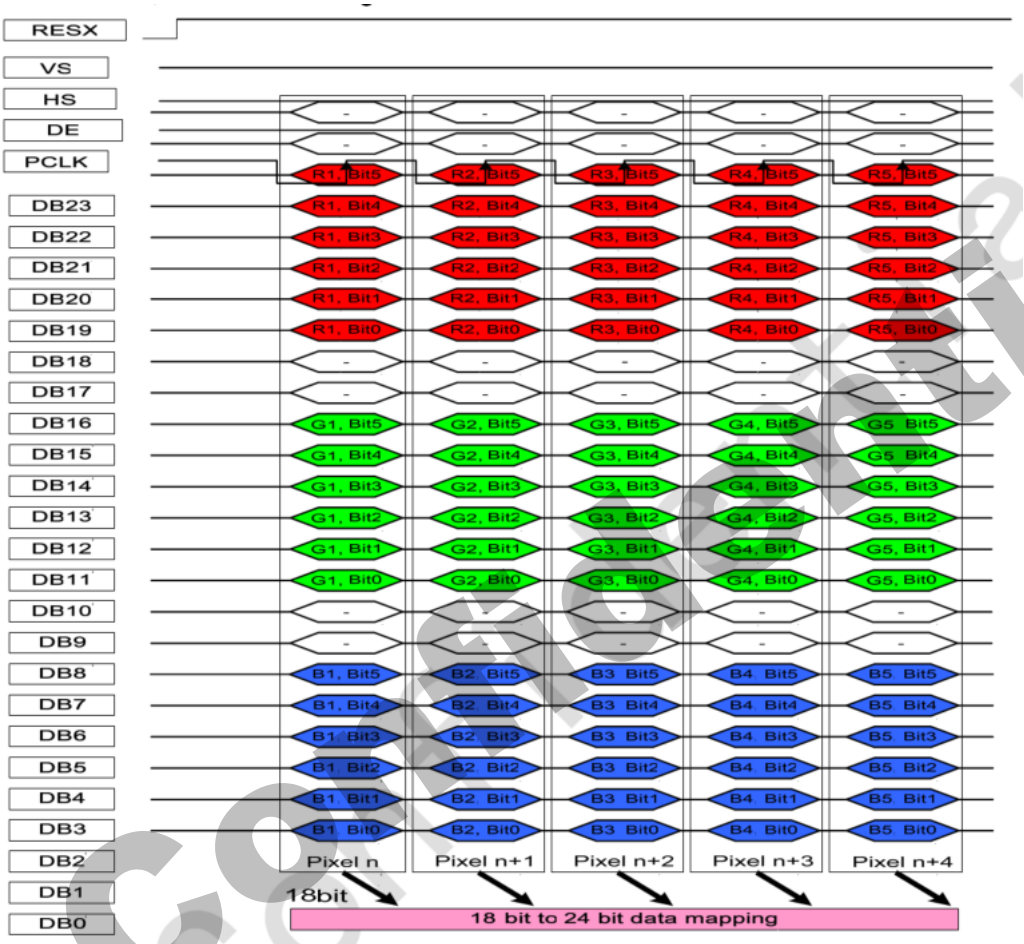


Figure 87 18-bit / pixel 262K colors order on the DPI Interface

Note:

The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.

1- times transfer is used to transmit 1 pixel data to the 18-bit color depth information.

2-

‘-‘= void

5.5.1.3 24-bit / pixel 16.7M colors order on the DPI Interface

The 24-bit RGB interface is selected by setting the DPI[2:0] bits to “111”. The display operation is synchronized with VS, HS and PCLK signals.

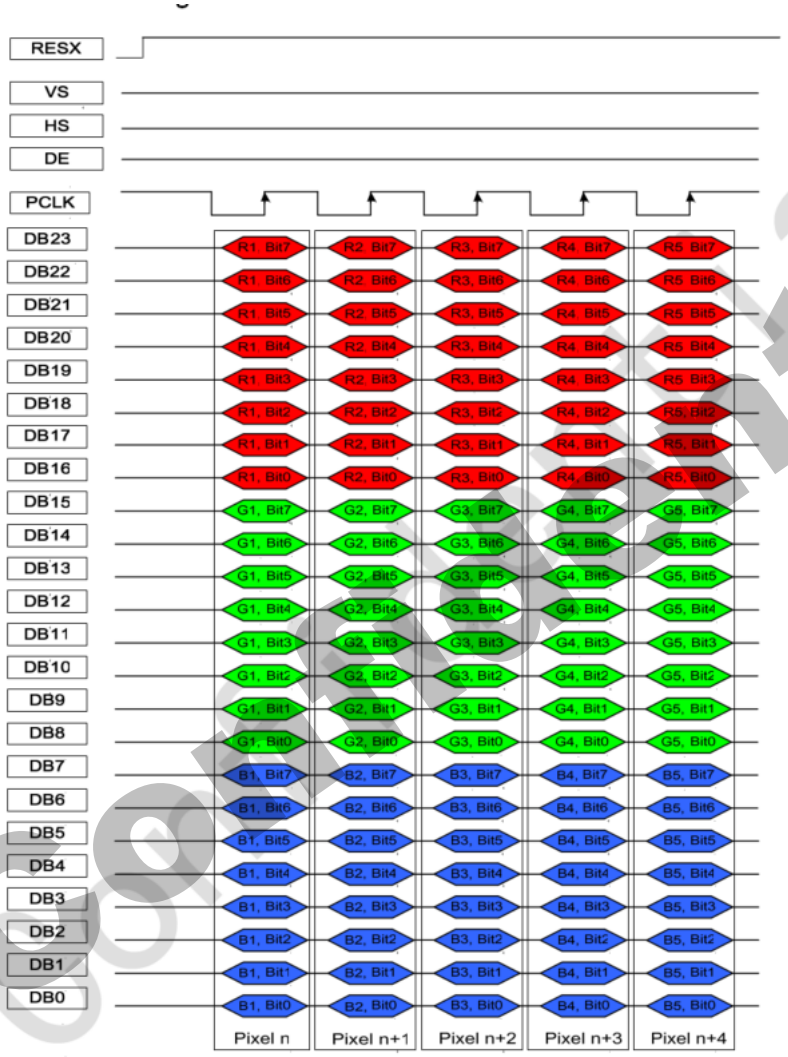


Figure 88 24-bit / pixel 16.7M colors order on the DPI Interface

Note :

The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 7, LSB=Bit 0 for Green, Red and Blue data.

1-times transfer is used to transmit 1 pixel data to the 24-bit color depth information.

5.5.2 DSI transmission data format

5.5.2.1 16-bit per Pixel, Long packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, GC9503NP has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

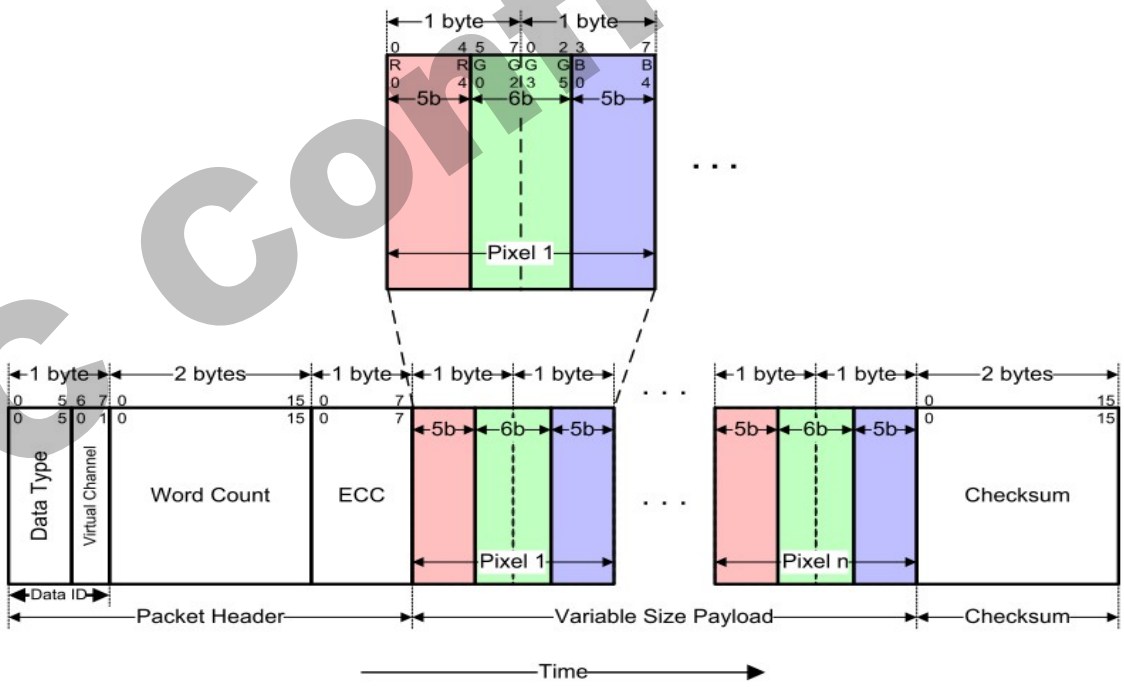


Figure 89 16-bit per Pixel, Data Type 00 1110 (0Eh)

5.5.2.2 18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

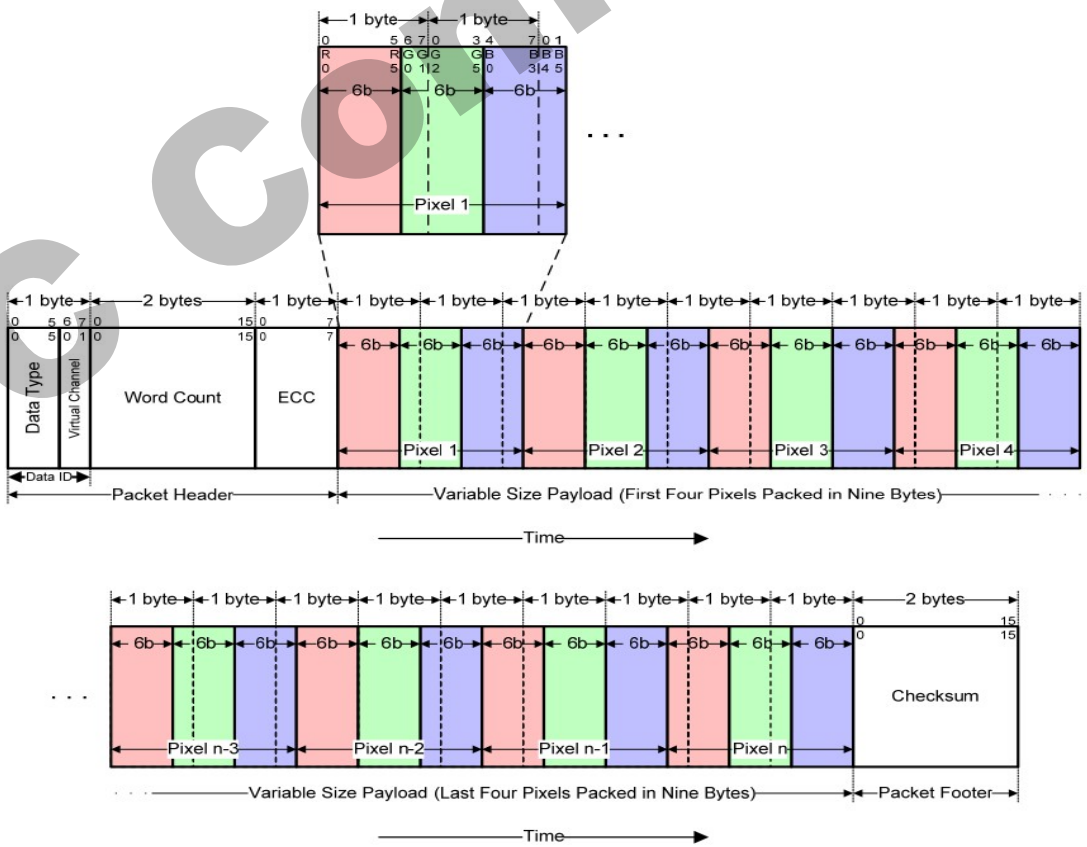


Figure 90 18-bit per Pixel, Data Type = 01 1110 (1Eh)

18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

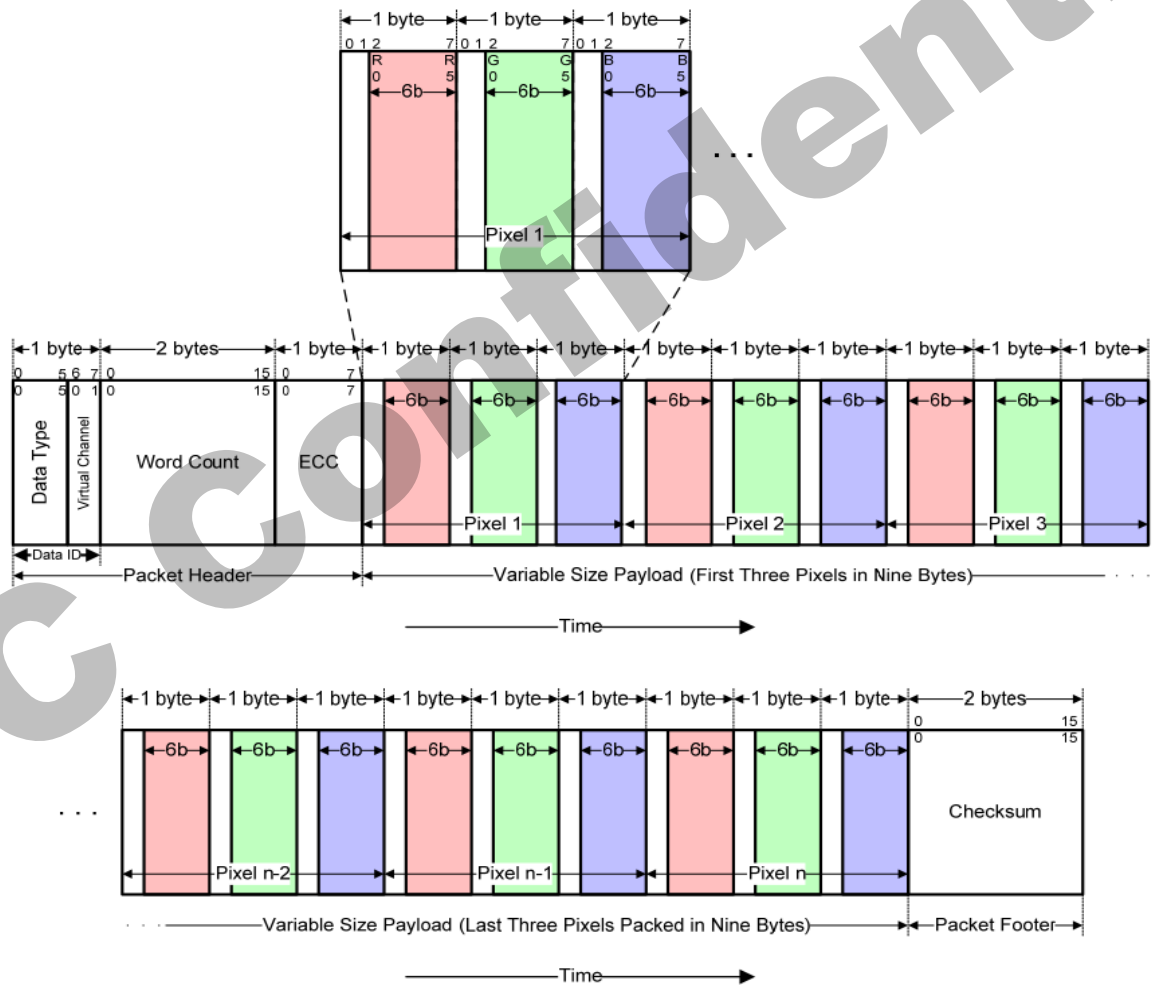


Figure 91 18-bit per Pixel, Data Type = 10 1110 (2Eh)

5.5.2.3 24-bit per Pixel, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

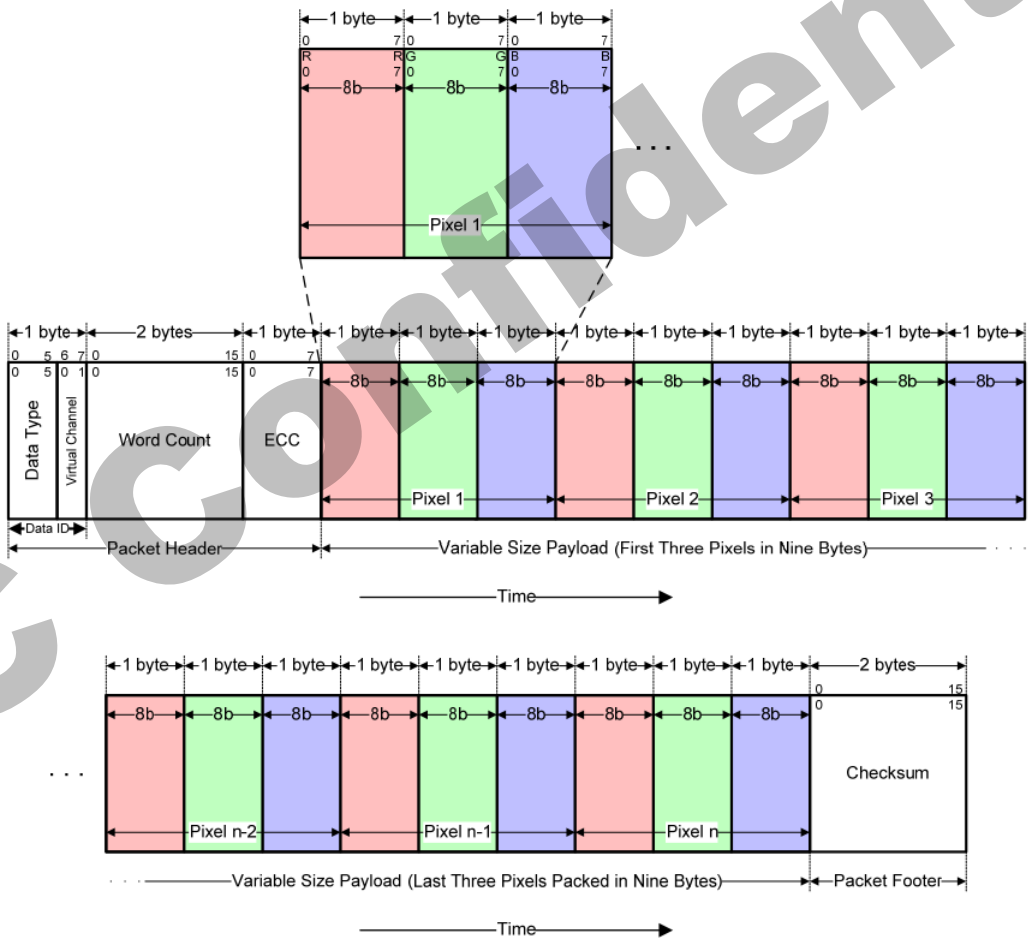


Figure 92 24-bit per Pixel, Data Type = 11 1110 (3Eh)

6 Command

6.1 User Command Set

Table 6.1.1 User Command Set

R/W	Address		Parameter										Function
	MIPI/spi8/9	Spi-16	D[15:8] (Non-MIPI/spi8/9)	D7	D6	D5	D4	D3	D2	D1	D0		
R	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read display ID
		0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
		0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
R	05h	0500h	00h	dsi_error[7:0]									RDNUMED
		0501h	00h	dsi_error[15:8]									
R	0Ah	0A00h	00h	sleep_out	idle	partial_on	sleep_out	normal_on	disp_on				Read Display Power Mode
R	0Bh	0B00h	00h				gs	bgr	ss				Read Display MADCTR
R	0Ch	0C00h	00h		vipf[2:0]								Read Display Pixel Format
R	0Dh	0D00h	00h			inv_on	pixel_on	pixel_off	gcs				Read Display Image Mode
W	10h	1000h	No Argument										Sleep in & booster off
W	11h	1100h	No Argument										Sleep out & booster on
W	12h	1200h	No Argument										Partial mode on
W	13h	1300h	No Argument										Normal display mode on
W	22h	2200h	No Argument										ALLPOFF
W	23h	2300h	No Argument										ALLPON
W	28h	2800h	No Argument										Display off
W	29h	2900h	No Argument										Display on
W	30h	3000h	00h							PSL9	PSL8		Partial start/end address set PSL[15:0]: partial start address PEL[15:0]: partial end address
		3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		3002h	00h							PEL9	PEL8		
		3003	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		

		h										
\W	38h	3800h	No Argument									Idle mode off
W	39h	3900h	No Argument									Idle mode on
W	3Ah	3A00h	00h		VIPF2	VIPF1	VIPF0					Interface pixel format
W	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness
R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness
W	53h	5300h	00h			BCTL				BL		Write Control Display
R	54h	5400h	00h			BCTL				BL		Read Control Display
R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
R	DBh	DB00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID2
R	DCh	DC00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID3
W	F0h	F000h	00h	0	1	0	1	0	1	0	1	Manufacture command enable
		F001h	00h	1	0	1	0	1	0	1	0	
		F002h	00h	0	1	0	1	0	0	1	0	
		F003h	00h	0	0	0	0	MAUNC	0	0	0	
		F004h	00h	0	0	0	0	0	0	0	PAGE	

Notes:

The 8-bit address code for "MIPI" in above table and following command description means include 3-wire 9-bit

6.1.1 Read Display ID (04h)

User Command Set		04h : RDNUMED (Read Display ID)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Read	ID1[7:0]								00h
2st Parameter	Read	ID2[7:0]								95h
3st Parameter	Read	ID3[7:0]								04h
Description	This read byte returns 24-bit display identification information. (the module's manufacture ID). And it is equal to returns value of Dah,DBh,DCh command.									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24'h009504</td></tr><tr><td>S/W Reset</td><td>24'h009504</td></tr><tr><td>H/W Reset</td><td>24'h009504</td></tr></table>									

6.1.2 Read DSI ERROR (05h)

User Command Set		05h : RDNUMED (Read DSI ERROR)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	0	1	0	1	05h
1st Parameter	Read	DSU_ERRO[7:0]								00h
2st Parameter	Read	DSU_ERRO[15:8]								00h

Description

This command returns an error report when DSI is used.
DSU_ERRO[15:0] is In accordance with Acknowledge with Error Report as followed.

DSU_ERRO	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error Y
4	Low-Power Transmit Sync Error Y
5	HS Receive Timeout Error
6	False Control Error
7	Reserved
8	ECC Error, single-bit (detected, and corrected) Y
9	ECC Error, multi-bit (detected, not corrected) Y
10	Checksum Error (Long packet only) Y
11	DSI Data Type Not Recognized Y
12	DSI VC ID Invalid Y
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	16'h0000
S/W Reset	16'h0000
H/W Reset	16'h0000

6.1.3 Read Display Power Mode (0Ah)

User Command Set		0Ah : RDDPM (Read Display Power Mode)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Read	booster	idle	partial_on	sleep_out	normal_on	disp_on	0	0	00h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or has a fault
		1	Booster On and working OK
D6	IDEL MODE	0	IDEL MODE ON
		1	IDEL MODE OFF
D5	PARTIAL MODE	0	PARTIAL MODE ON
		1	PARTIAL MODE O
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/ Off	0	Display Normal Mode Off.
		1	Display Normal Mode On
D2	Display On/Off	0	Display is Off.
		1	Display is On

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

6.1.4 Read Display MADCTL (0Bh)

User Command Set		0Bh : RDDPM (Read Display Power Mode)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	0	1	1	0Bh
1st Parameter	Read	0	0	0	0	BGR	0	GS	SS	00h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D7	Reserved	0	Reserved, so it is set to '0'
D6	Reserved	0	Reserved, so it is set to '0'
D5	Reserved	0	Reserved, so it is set to '0'
D4	Reserved	0	Reserved, so it is set to '0'
D3	BGR	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1').
D2	Reserved	0	Reserved, so it is set to '0'
D1	GS	0	Gate output Top to Bottom
		1	Gate output Bottom to Top
D0	SS	0	Source output Left to Right
		1	Source output Right to Left

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

6.1.5 Read Display Pixel Format (0Ch)

User Command Set		0Ch : RDDPM (Read Display Pixel Format)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	1	0	0	0Ch
1st Parameter	Read	0	VIPF2	VIPF 1	VIFP 0	0	0	0	0	70h

Description

This command indicates the current status of the display as described in the table below.

VIPF[2:0]			RGB Interface Format
1	0	1	16-bit / pixel
1	1	0	18-bit / pixel
1	1	1	24-bit / pixel
Others			Reserved

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h70
H/W Reset	8'h70

6.1.6 Read Display Image Mode (0Dh)

User Command Set		0Dh : RDDPM (Read Display Image Mode)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	0	1	1	0	1	0Dh
1st Parameter	Read	0	0	INVO	allpo	allpoff	0	0	0	00h

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value	Status
D5	Inversion On/Off	0	Inversion is Off.
		1	Inversion is On.
D4	All Pixels On	0	Normal Display
		1	White Display
D3	All Pixels Off	0	Normal Display
		1	Black Display

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

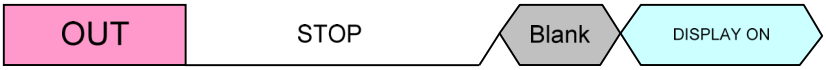
Default

Status	Default Value
Power On Sequence	According to initial code
S/W Reset	8'h00
H/W Reset	8'h00

6.1.7 Sleep In (10h)

User Command Set		10h : CLOMD(Sleep In)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	0	0	10h
1st Parameter	-	xx								XXh
Description	This command causes the GC9503NP to enter the minimum power consumption mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep out mode</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table>									

6.1.8 Sleep Out (11h)

User Command Set		11h : CLOMD(Sleep Out)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	0	1	11h
1st Parameter	-	xx								XXh
Description	This command causes the GC9503NP to enter the Sleep Out mode 									
Restriction	This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The GC9503NP loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the GC9503NP is already Sleep Out mode.									
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Sleep out mode
S/W Reset	Sleep in mode
H/W Reset	Sleep in mode

6.1.9 Partial Mode On (12h)

User Command Set		12h :CLOMD(Partial Mode On)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	1	0	12h
1st Parameter	-	xx								XXh
Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) To leave Partial mode, the Normal Display Mode On command (13H) should be written. There is no abnormal visual effect during mode change between Normal mode On to Partial									
Restriction	This command has no effect when Normal Display Mode is active.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

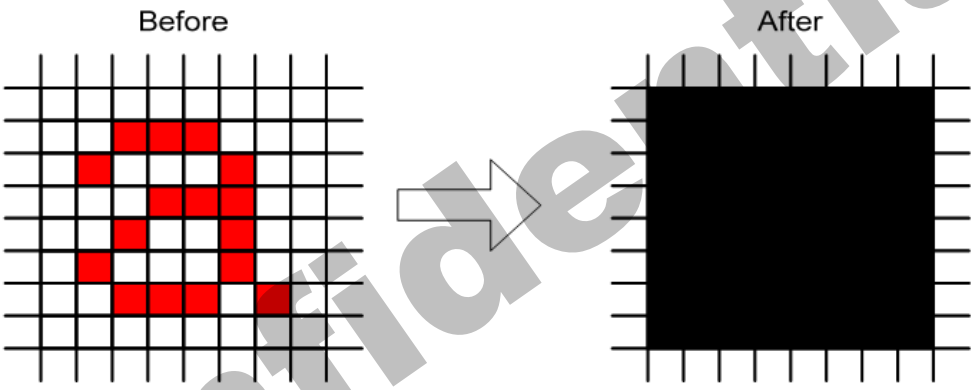
6.1.10 Normal Display Mode On (13h)

User Command Set		13h :CLOMD(Normal Display Mode On)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	0	1	0	0	1	1	13h
1st Parameter	Read	xx								XXh
Description	This command returns the display to Normal Display									
Restriction	This command has no effect when Normal Display Mode is active.									
Register Availability										
Default										

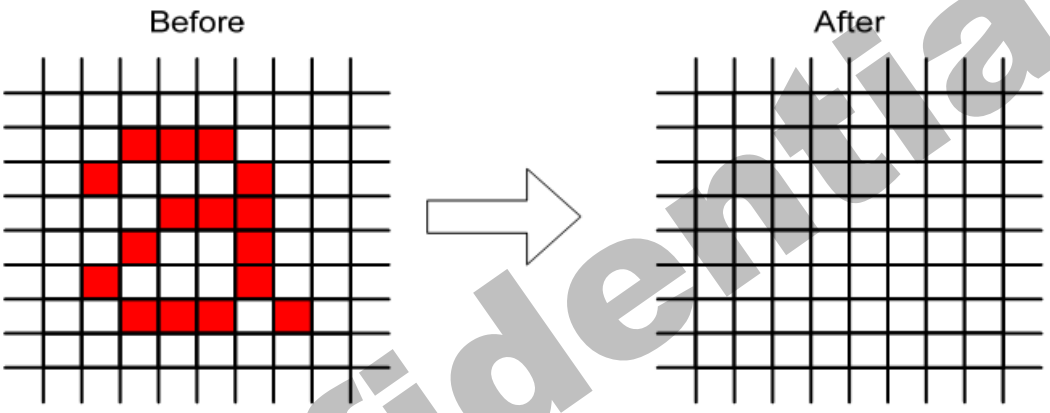
Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Normal display mode on
S/W Reset	Normal display mode on
H/W Reset	Normal display mode on

6.1.11 All Pixel Off (22h)

User Command Set		22h : CLOMD(all pixel Off)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	-	xx								XXh
Description	This command turns the display panel black in 'Sleep Out' mode and a status of the' Display On/Off' register can be 'on' or 'off'. This command does not change any other status 'All Pixels On', 'Normal Display Mode On' commands are used to leave this mode. 									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display inversion off</td></tr><tr><td>S/W Reset</td><td>Display inversion off</td></tr><tr><td>H/W Reset</td><td>Display inversion off</td></tr></table>									

6.1.12 All Pixel On (23h)

User Command Set		23h : CLOMD(all pixel On)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	Read	xx								XXh
Description	This command turns the display panel white in 'Sleep Out ' mode and a status of the 'Display On/Off' register can be 'on' or 'off'. This command does not change any other status. 'All Pixels Off', 'Normal Display Mode On'– commands are used to leave this mode. 									
Restriction										

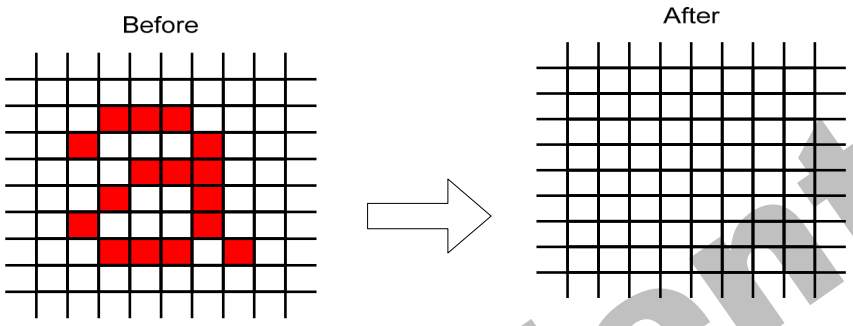
Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display inversion off
S/W Reset	Display inversion off
H/W Reset	Display inversion off

6.1.13 Display Off (28h)

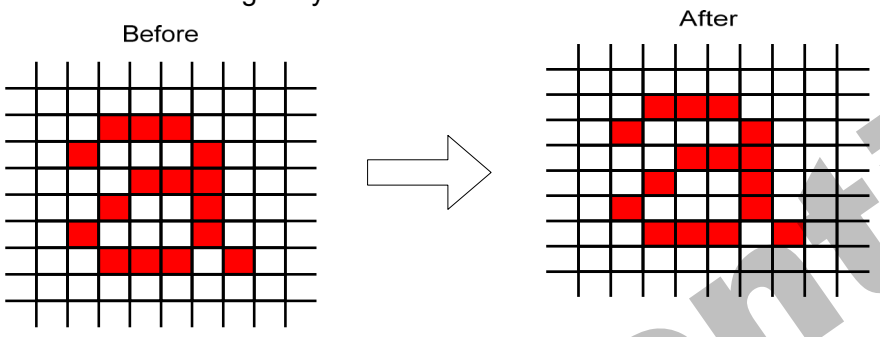
User Command Set		28h : CLOMD(Display Off)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	1	0	0	0	28h
1st Parameter	-	xx								XXh
Description	This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted. This command makes no change any other status. There will be no abnormal visible effect on the display. 									
Restriction	This command has no effect when module is already in Display Off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	display on mode
S/W Reset	display off mode
H/W Reset	display off mode

6.1.14 Display ON (29h)

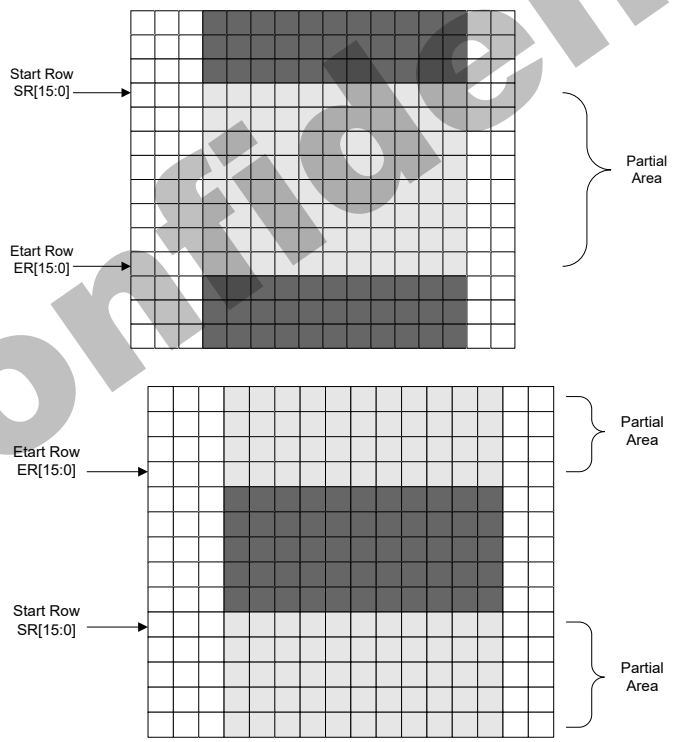
User Command Set		29h : CLOMD(Display On)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	1	0	0	1	29h
1st Parameter	-	xx								XXh
Description	This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status. 									
Restriction	This command has no effect when the GC9503NP is already in Display on mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	display on mode
S/W Reset	display off mode
H/W Reset	display off mode

6.1.15 Partial Area (30h)

User Command Set		30h : CLOMD(Partial Area)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	1	0	0	0	0	30h
1stParameter	Write							PSL9	PSL8	00h
2stParameter	Write	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	00h
3stParameter	Write							PEL9	PEL8	00h
4stParameter	Write	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	00h
Description	This command returns the display to Normal Display									
Restriction	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.  If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	32'h00000000
S/W Reset	32'h00000000
H/W Reset	32'h00000000

6.1.16 Idle Mode Off (38h)

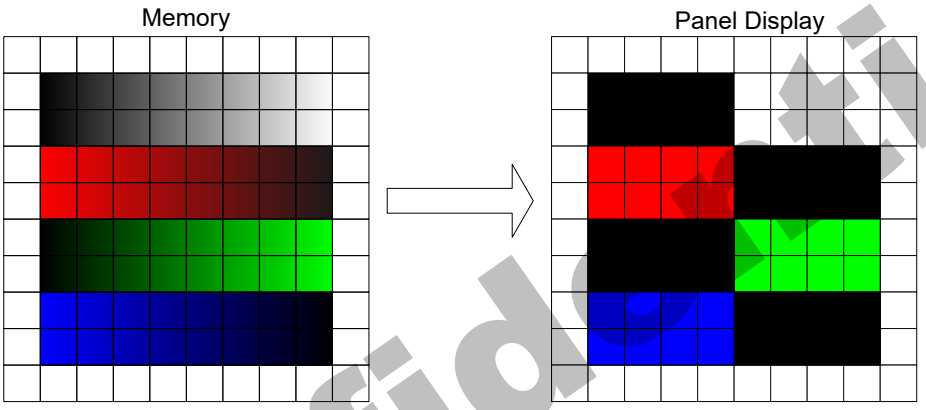
User Command Set		38h : CLOMD(Idle Mode Off)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	1	1	0	0	0	38h
1st Parameter	-	xx								xxh
Description	This command returns the display to Normal Display									
Restriction	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colors. X = Don't care.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
S/W Reset	Idle mode OFF
H/W Reset	Idle mode OFF

6.1.17 Idle Mode On (39h)

User Command Set		39h : CLOMD(Idle Mode On)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	1	1	0	0	1	39h
1st Parameter	Write	xx								xxh
Description	This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. 									
Restriction	This command has no effect when module is already in idle off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
S/W Reset	Idle mode OFF
H/W Reset	Idle mode OFF

6.1.18 Interface Pixel Format (3Ah)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">3Ah : COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Wr</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3ah</td></tr>
<tr><td>1stParamete</td><td>Wr</td><td>0</td><td colspan="3">VIPF[2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70h</td></tr>
<tr><td>Description</td><td colspan="10">This command sets the pixel format. VIPF[2:0] selects the pixel format of RGB interface.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24-bit / pixel</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h70</td></tr>
<tr><td>S/W Reset</td><td>8’h70</td></tr>
<tr><td>H/W Reset</td><td>8’h70</td></tr>
</table></td></tr>
</table>

6.1.19 Write Display Brightness Value (51h)

User Command Set		51h : COLMOD (Interface Pixel Format)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write	0	DBV[7:0]							00h
Description	The command is used to adjust the brightness value of the display. DBV[7:0]: 8 bit, for display brightness of manual brightness setting in the GC9503NP. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.									
Restriction										
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table>									

6.1.20 Read Display Brightness Value (52h)

User Command Set		52h : COLMOD (Interface Pixel Format)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	1	0	1	0	52h
1st Parameter	Write	0	DBV[7:0] 0 0 0 0							00h
Description	The command is used to read the brightness value of the display. DBV[7:0]: 8 bit, for display brightness of manual brightness setting in the GC9503NP. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

6.1.21 Write CTL Display(53h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">53h : COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53hh</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>0</td><td>0</td><td>BCTRL</td><td>0</td><td>0</td><td>BL</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to control ambient light, brightness and gamma setting.
BCTRL: Brightness Control Block On/Off
The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

<table>
<tr><th>BCTRL</th><th>DESCRIPTION</th><th>LEDPWM Pin</th></tr>
<tr><td>0</td><td>Off,
DBV[7:0] are 00h.</td><td>LEDPWPOL=”0”: keep low (0%, high level is duty)
LEDPWPOL=”1”: keep high (0%, low level is duty)</td></tr>
<tr><td>1</td><td>On,
DBV[7:0] are active</td><td>LEDPWPOL=”0”: PWM output (high level is duty)
LEDPWPOL=”1”: PWM output (low level is duty)</td></tr>
</table>

BL: Backlight Control On/Off without Dimming Effect
When BL bit change from “On” to “Off”, display brightness is turned off without gradual dimming, even if
dimming on (DD=”1”) is selected.
<table>
<tr><th>BL</th><th>DESCRIPTION</th><th>LEDON Pin</th></tr>
<tr><td>0</td><td>Off</td><td>LEDONPOL=”0”: output low (for high active)
LEDONPOL=”1”: output high (for low active)</td></tr>
<tr><td>1</td><td>on</td><td>LEDONPOL=”0”: output high (for high active)
LEDONPOL=”1”: output low (for low active)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>Default</td>
<td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table>
</td>
</tr>
</table>

6.1.22 Read CTL Display(54h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">54h : COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Writee</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>54h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>BCTRL</td><td>0</td><td>0</td><td>BL</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="10">This command returns ambient light, brightness control and gamma setting value.
BCTRL: Brightness Control Block On/Off
The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

<table>
<tr><th>BCTRL</th><th>DESCRIPTION</th><th>LEDPWM Pin</th></tr>
<tr><td>0</td><td>Off,
DBV[7:0] are 00h.</td><td>LEDPWPOL=”0”: keep low (0%, high level is duty)
LEDPWPOL=”1”: keep high (0%, low level is duty)</td></tr>
<tr><td>1</td><td>On,
DBV[7:0] are active</td><td>LEDPWPOL=”0”: PWM output (high level is duty)
LEDPWPOL=”1”: PWM output (low level is duty)</td></tr>
</table>

BL: Backlight Control On/Off without Dimming Effect
When BL bit change from “On” to “Off”, display brightness is turned off without gradual dimming, even if
dimming on (DD=”1”) is selected.
<table>
<tr><th>BL</th><th>DESCRIPTION</th><th>LEDON Pin</th></tr>
<tr><td>0</td><td>Off</td><td>LEDONPOL=”0”: output low (for high active)
LEDONPOL=”1”: output high (for low active)</td></tr>
<tr><td>1</td><td>on</td><td>LEDONPOL=”0”: output high (for high active)
LEDONPOL=”1”: output low (for low active)</td></tr>
</table>

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at
DD=”1”, e.g. BCTRL: 0_1 or 1_0.
Note: All read and write commands are valid, but there is no effect (except registers can be changed)
when write commands are used.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
</table>

6.1.23 Read ID1 (DAh)

User Command Set		DAh : RDDPM (Read ID1)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	1	1	0	1	1	0	1	0	DAh
1st Parameter	Read	ID1[7:0]								8h'00
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 1rst parameter of 04h command. The ID1 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0h'00
S/W Reset	0h'00
H/W Reset	0h'00

6.1.24 Read ID2 (DBh)

User Command Set		DBh : RDDPM (Read ID2)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	1	1	0	1	1	0	1	1	DBh
1st Parameter	Read	ID2[7:0]								8'h95
Description	This read byte returns 8-bit display identification information. (the module's manufacture ID). And it is equal to returns 2th parameter of 04h command. The ID2 is programmed by OTP function.									
Restriction										
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0'h95
S/W Reset	0'h95
H/W Reset	0'h95

6.1.25 Read ID3 (DCh)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">DCh : RDDPM (Read ID3)</th></tr>
<tr><td colspan="2"></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">ID3[7:0]</td><td>8’h04</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns 8-bit display identification information. (the module’s manufacture ID). And it is equal to returns 3th parameter of 04h command.
The ID3 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h04</td></tr><tr><td>S/W Reset</td><td>8’h04</td></tr><tr><td>H/W Reset</td><td>8’h04</td></tr></table></td></tr>
</table>

6.1.26 EXTC Command Set enable register (F0h)

User Command Set		F0h : COLMOD (EXTC Command Set enable register)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	1	1	1	1	0	0	0	0	F0h
1st Parameter	Write	0	1	0	1	0	1	0	1	55h
2st Parameter	Write	1	0	1	0	1	0	1	0	aah
3st Parameter	Write	0	1	0	1	0	0	1	0	52h
4st Parameter	Write	0	0	0	0	MAUNC	0	0	0	08h
5st Parameter	Write	0	0	0	0	0	0	0	PAGE	00h

Description

Bit	Description	Value
MAUC	Manufacture Command Set enable/disable	“0”: Manufacture Command Set disable “1”: Manufacture Command Set enable
PAGE	Manufacture Command Set selection	“0”: Page 0
		“1”: Page 1

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	40h’55aa520800
S/W Reset	40h’55aa520800
H/W Reset	40h’55aa520800

6.2 Page 0 Command Set

Table 6.1.2 Page 0 Command Set

R/W	Address		Parameter									Function
	MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
W	80h	8000h	00h	D2D_VOFFSET[7:0]								VREG_CTL0
W	82h	8200h	00h	D2D_VGSPN_AD_TMP1[7:0]								VREG_CTL1
		8201h	00h	D2D_VGSPN_AD_TMP2[7:0]								
W	86h	8600h	00h	0x99								CHP_CTL1
		8601h	00h	0Xa3								
W	82h	8602h	00h	0xa3								
		8603h	00h	0	D2A_VGL_AD[2:0]			0	0	0	1	
W	98h	9800h	00h	D2D_VREG_VGMP_AD_TMP1[7:0]								VREG_CTL2
W	99h	9900h	00h	D2D_VREG_VGMN_AD_TMP1[7:0]								VREG_CTL3
W	9Ah	9A00h	00h	D2D_VREG_VGMP_AD_TMP2[7:0]								VREG_CTL4
W	9Bh	9B00h	00h	D2D_VREG_VGMN_AD_TMP2[7:0]								VREG_CTL5
W	A0h	A000h	00h	D2D_VGHS[3:0]_TMP1				D2D_VGHS[3:0]_TMP2				CHP_CTL5
W	C4h	C400h	00h		reg_en_86 (0)				reg_en_82 (1)		reg_en_80 (1)	REG_CTL1
W	C7h	C700h	00h					reg_en_9B (1)	reg_en_9A (1)	reg_en_99 (0)	reg_en_98 (0)	REG_CTL4
W	C8h	C800h	00h							reg_en_a1 (0)	reg_en_a0 (0)	REG_CTL5
W	B0h	B000h	00h	rgb_mode				PCKP	DEP	HSP	VSP	RGB_MODE
		B001h	00h	VBP[7:0]								RGB_MODE
		B002h	00h	VFP[7:0]								
		B003h	00h	HBP[7:0]								
		B004h	00h	HFP[7:0]								
W	B1h	B100h	00h	REV		BGR	NLA[2:0](dinv)	GS	SS			Display_CTL

6.2.1 VREG_CTL0 (80h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><th></th><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>80h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VOFFSET[7:0]</td><td>8’h00</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VOFFSET is the offset of VGMP and VGSPN and VGMN together, which is used to dispel the flicker.
<table>
<tr><th>D2D_VOFFSET[7:0]</th><th>Offset of VREG</th><th>D2D_VOFFSET[7:0]</th><th>Offset of VREG</th></tr>
<tr><td>0</td><td>+0</td><td>128</td><td>-127</td></tr>
<tr><td>1</td><td>+1</td><td>129</td><td>-126</td></tr>
<tr><td>..</td><td>…</td><td>..</td><td>..</td></tr>
<tr><td>..</td><td>…</td><td>..</td><td>..</td></tr>
<tr><td>126</td><td>+126</td><td>254</td><td>-1</td></tr>
<tr><td>127</td><td>+127</td><td>255</td><td>-0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (C4h)” b0” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

6.2.2 VREG_CTL1 (82h)

User Command Set										
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	82h
1st Parameter	Write	D2D_VGSPN_AD_TMP1[7:0]								8'h4f
2th Parameter	Write	D2D_VGSPN_AD_TMP2[7:0]								8'h4f

Description

D2D_VGSPN_AD_TMP 1 is the adjustment register of VGSPN in low-temperature environment.
D2D_VGSPN_AD_TMP 2 is the adjustment register of VGSPN in normal-temperature environment.

D2D_VGSPN_AD_TMP 1[7:0]	VGSPN(V)	D2D_VGSPN_AD_TMP 2[7:0]	VGSPN(V)
0	0.0125	0	0.0125
1	0.0250	1	0.0250
2	0.0375	2	0.0375
..	…	..	…
n	(n+1)*0.0125	n	(n+1)*0.0125
..	…	..	…
199	2.5	199	2.5
200	inhibited	200	inhibited
…	inhibited	…	inhibited
255	inhibited	255	inhibited

Restriction

To enable this command, "Page 0 Command Set enable register (F0h) " must set first. And enable register (C4h)" b2" must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	16'h4f4f
S/W Reset	16'h4f4f
H/W Reset	16'h4f4f

6.2.3 CHP_CTL1 (86h)

User Command Set		CHP_CTL1								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	86h
1stParameter	Write	0x99								0x99
2thParameter	Write	0Xa3								0Xa3
3thParameter	Write	0xa3								0xa3
4thParameter	Write	0	D2A_VGL_AD[2:0]			0	0	0	1	0x21

Description

D2A_VGL_AD the adjustment register of VGL amplitude.

D2A_VGL_AD[2:0]	VGL(V)
0	-8.0
1	-8.5
2	-9.0
3	-9.5
4	-10.0
5	-10.5
6	-11.0
7	-11.5

Restriction

To enable this command, “Page 0 Command Set enable register (F0h) ” must set first. And enable register (C4h)” b6” must set 1

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32’h99a3a321
S/W Reset	32’h99a3a321
H/W Reset	32’h99a3a321

6.2.4 VREG_CTL2 (98h)

<table>
<tr><td colspan="2">User Command Set</td><td colspan="9"></td></tr>
<tr><td></td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>98h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMP_AD_TMP1[7:0]</td><td>8’Hc2</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMP_AD_TMP 1 is the adjustment register of VGMP in low-temperature environment.
<table>
<tr><th>D2D_VREG_VGMP_AD_TMP1[7:0]</th><th>VGMP(V)</th></tr>
<tr><td>0</td><td>3.575</td></tr>
<tr><td>1</td><td>3.5875</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>N</td><td>3.575+0.0125*N</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>217</td><td>6.2875</td></tr>
<tr><td>…</td><td>inhibited</td></tr>
<tr><td>255</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (C7h)” b0” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’hc2</td></tr>
<tr><td>S/W Reset</td><td>8’hc2</td></tr>
<tr><td>H/W Reset</td><td>8’hc2</td></tr>
</table></td></tr>
</table>

6.2.5 VREG_CTL3 (99h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><th></th><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>99h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMN_AD_TMP1[7:0]</td><td>8’H4a</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMN_AD_TMP1 is the adjustment register of VGMN in low-temperature environment.
<table>
<tr><th>D2D_VREG_VGMN_AD_TMP1[7:0]</th><th>VGMN(V)</th></tr>
<tr><td>0</td><td>inhibited</td></tr>
<tr><td>..</td><td>inhibited</td></tr>
<tr><td>50</td><td>-4.300</td></tr>
<tr><td>51</td><td>-4.2875</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>N</td><td>-4.3+(N-50)*0.0125</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>255</td><td>-1.7375</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (C7h)” b1” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h4a</td></tr>
<tr><td>S/W Reset</td><td>8’h4a</td></tr>
<tr><td>H/W Reset</td><td>8’h4a</td></tr>
</table></td></tr>
</table>

6.2.6 VREG_CTL4 (9Ah)

<table>
<tr><td colspan="2">User Command Set</td><td colspan="9"></td></tr>
<tr><td></td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>9Ah</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMP_AD_TMP2[7:0]</td><td>8’Hc2</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMP_AD_TMP 2 is the adjustment register of VGMP in normal-temperature environment.
<table>
<tr><th>D2D_VREG_VGMP_AD_TMP2[7:0]</th><th>VGMP(V)</th></tr>
<tr><td>0</td><td>3.575</td></tr>
<tr><td>1</td><td>3.5875</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>N</td><td>3.575+0.0125*N</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>217</td><td>6.2875</td></tr>
<tr><td>…</td><td>inhibited</td></tr>
<tr><td>255</td><td>inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first. And enable register (C7h)” b2” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’hc2</td></tr>
<tr><td>S/W Reset</td><td>8’hc2</td></tr>
<tr><td>H/W Reset</td><td>8’hc2</td></tr>
</table></td></tr>
</table>

6.2.7 VREG_CTL5 (9Bh)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9"></th></tr>
<tr><th></th><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>9Bh</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">D2D_VREG_VGMN_AD_TMP2[7:0]</td><td>8’H4a</td></tr>
<tr><td>Description</td><td colspan="10">D2D_VGMN_AD_TMP2 is the adjustment register of VGMN in normal-temperature environment.
<table>
<tr><th>D2D_VREG_VGMN_AD_TMP2[7:0]</th><th>VGMN(V)</th></tr>
<tr><td>0</td><td>inhibited</td></tr>
<tr><td>..</td><td>inhibited</td></tr>
<tr><td>50</td><td>-4.300</td></tr>
<tr><td>51</td><td>-4.2875</td></tr>
<tr><td>..</td><td>…</td></tr>
<tr><td>N</td><td>-4.3+(N-50)*0.0125</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>255</td><td>-1.7375</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (C7h)” b3” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h4a</td></tr>
<tr><td>S/W Reset</td><td>8’h4a</td></tr>
<tr><td>H/W Reset</td><td>8’h4a</td></tr>
</table></td></tr>
</table>

6.2.8 CHP_CTL5(A0h)

<table>
<tr><th colspan="2">User Command Set</th><th colspan="9">7Fh : CHP_CTL6</th></tr>
<tr><td></td><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>A0h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="5">D2D_VGHS_TMP1[3:0]</td><td colspan="4">D2D_VGHS_TMP2[3:0]</td><td>8’h77</td></tr>
<tr><td>Description</td><td colspan="10">D2D_ VGHS _TMP1 is the adjustment register of VGH in low-temperature environment.
D2D_ VGHS _TMP2 is the adjustment register of VGH in normal-temperature environment.
<table>
<tr><th>D2D_VGHS_TMP1[3:0]</th><th>VGH(V)</th><th>D2D_VGHS_TMP2[3:0]]</th><th>VGH(V)</th></tr>
<tr><td>0</td><td>8.47</td><td>0</td><td>8.47</td></tr>
<tr><td>1</td><td>9.00</td><td>1</td><td>9.00</td></tr>
<tr><td>2</td><td>9.47</td><td>2</td><td>9.47</td></tr>
<tr><td>3</td><td>10.00</td><td>3</td><td>10.00</td></tr>
<tr><td>4</td><td>10.43</td><td>4</td><td>10.43</td></tr>
<tr><td>5</td><td>11.07</td><td>5</td><td>11.07</td></tr>
<tr><td>6</td><td>11.43</td><td>6</td><td>11.43</td></tr>
<tr><td>7</td><td>12.00</td><td>7</td><td>12.00</td></tr>
<tr><td>8</td><td>12.41</td><td>8</td><td>12.41</td></tr>
<tr><td>9</td><td>13.09</td><td>9</td><td>13.09</td></tr>
<tr><td>10</td><td>13.58</td><td>10</td><td>13.58</td></tr>
<tr><td>11</td><td>14.12</td><td>11</td><td>14.12</td></tr>
<tr><td>12</td><td>14.40</td><td>12</td><td>14.40</td></tr>
<tr><td>13</td><td>15.00</td><td>13</td><td>15.00</td></tr>
<tr><td>14</td><td>15.65</td><td>14</td><td>15.65</td></tr>
<tr><td>15</td><td>16.00</td><td>15</td><td>16.00</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (F0h) ” must set first.
And enable register (C8h)” b1” must set 1</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h77</td></tr>
<tr><td>S/W Reset</td><td>8’h77</td></tr>
<tr><td>H/W Reset</td><td>8’h77</td></tr>
</table></td></tr>
</table>

6.2.9 RGB Interface Signals Control(B0h)

User Command Set		B0h : RGB Interface Signals Control								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	B0h
1st Parameter	Write	CMRC				PCKP	DEP	HSP	VSP	00h
2th Parameter	Write	VBP[7:0]								0Eh
3th Parameter	Write	VFP[7:0]								0Eh
4th Parameter	Write	HBP[7:0]								14h
5th Parameter	Write	HFP[7:0]								04h

Description

Bit	Description	Value
CRCM	Select the RGB mode1/mode 2	“0” = RGB mode 1(DE mode)
		“1” = RGB mode 2(Sync mode)
PCKP	PCLK Fetch Polarity	“0” = Data latched at the rising edge of PCLK
		“1” = Data latched at the falling edge of PCLK
DEP	DE Enable Polarity	“0” = High enable for RGB interface
		“1” = Low enable for RGB interface
HSP	H-Sync Pulse Level	“0” = Low pulse level sync clock
		“1” = High pulse level sync clock
VSP	V-Sync Pulse Level	“0” = Low pulse level sync clock
		“1” = High pulse level sync clock
VBP[7:0]	V-Sync Back Porch	“05h” to “FFh” = 5 to 255 H-Sync clocks
VFP[7:0]	V-Sync Front Porch	“02h” to “FFh” = 2 to 255 H-Sync clocks
HBP[7:0]	H-Sync Back Porch	“05h” to “FFh” = 5 to 255 PCLK clocks
HFP[7:0]	H-Sync Front Porch	“02h” to “FFh” = 2 to 255 PCLK clocks

The registers VBP[7:0], VFP[7:0], HBP[7:0] and HFP[7:0] for vertical and horizontal porch control are used in RGB interface mode 2 only. The setting value “00h” is invalid for all of these four registers.

RGB IF Mode	PCLK	DE	D[23:0]	VS	HS	VBP[7:0], VFP[7:0], HBP[7:0], HFP[7:0]
RGB Mode 1	Used	Used	Used	Used	Used	Not Used
RGB Mode 2	Used	Not Used	Used	Used	Used	Used

Restriction

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	B000h	B001h	B002h	B003h	B004h
Power On Sequence	00h	0Eh	0Eh	14h	04h
S/W Reset	00h	0Eh	0Eh	14h	04h
H/W Reset	00h	0Eh	0Eh	14h	04h

6.2.10 DISPLAY_CTL (B1h)

User Command Set		BCh : COLMOD (Display Inversion Control)								
		D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	D7	D6	D5	D4	D3	D2	D1	D0	B1h
1st Paramete	Write	REV	0	BGR	NLA[2:0](dinv)			GS	SS	10h

Description

REV=0
recover from Display Inversion On mode

REV=1
enter into Display Inversion On mode

BGR=0
BGR color filter panel

BGR=1
RGB color filter panel

GS: Select the Gate driver scan direction on panel module
SS:Select the Source driver scan direction on panel module

NLA[2:0]	Inersion Mode for Source Driver
000	1-Dot inversion
001	2-Dot inversion
010	3-Dot inversion
011	4-Dot inversion
100	Column inversion
101-111	reserved

Restrictio

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h10
S/W Reset	8'h10
H/W Reset	8'h10

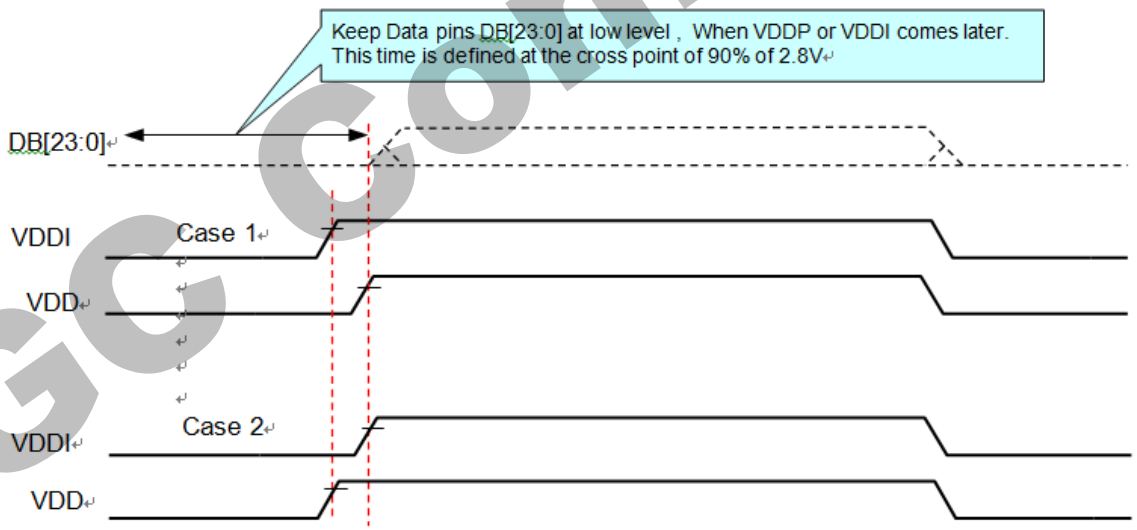
7 Power ON/OFF Sequence

VDDI and VDD can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VDD and VDDI can be powered down with minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

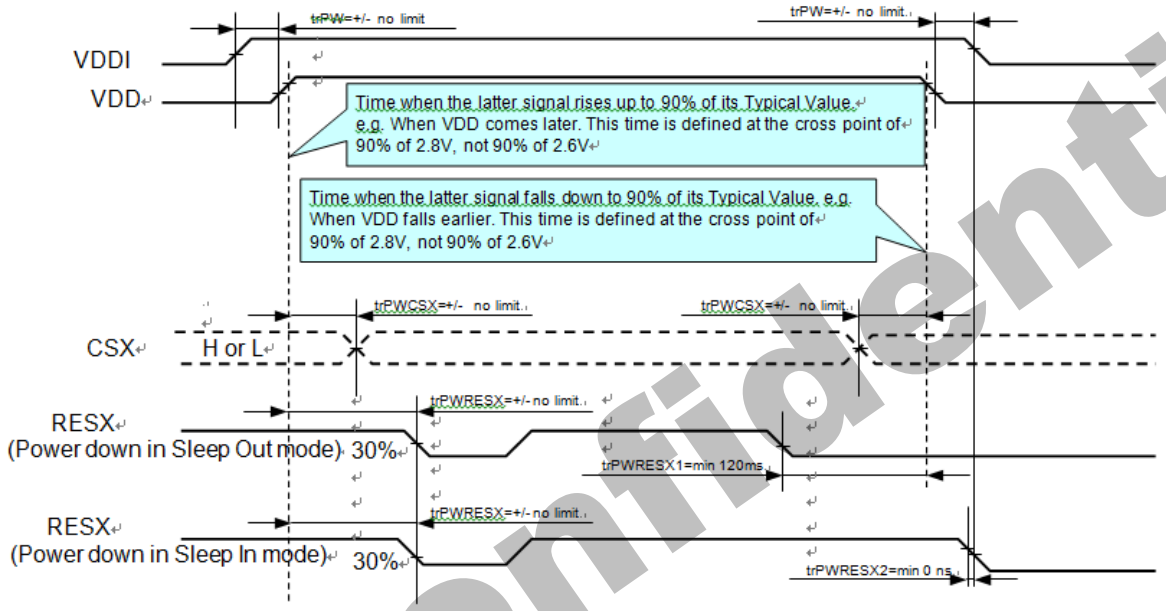
Note:

1. There will be no damage to GC9503NP if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VDD or VDDI comes later



7.1 Case 1 –RESX line is held High or Unstable by Host at Power ON

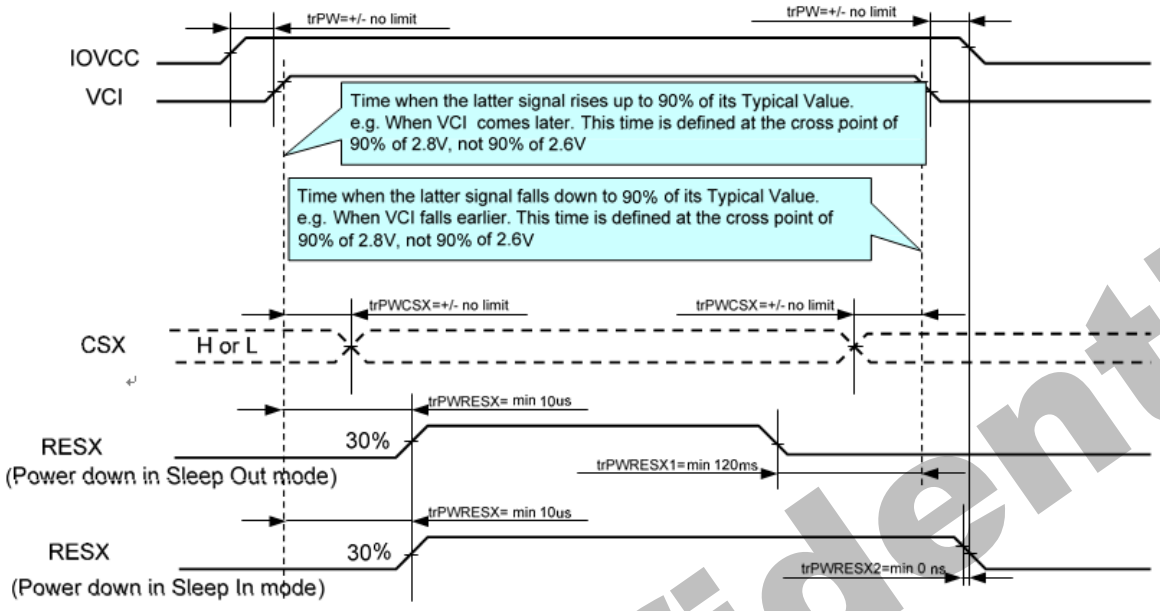
If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no
timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

7.2 Case 2 – RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD and VDDI have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Figure 99 Case 2 – RESX line is held Low by Host at Power ON

Note: 1. Unless otherwise specified, timings herein show cross point at 50% of signal power level.

7.3 Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9503NP will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on Table 42. When the GC9503NP is used out of the absolute maximum ratings, it may be permanently damaged. To use the GC9503NP within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the GC9503NP will malfunction and cause poor reliability.

Table 43 Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VDD ~ AGND	V	-0.3 ~ +4.6
Supply voltage (I/O)	VDDI ~ DGND	V	-0.3 ~ +4.6
OTP Supply voltage	VPP ~ AGND	V	-0.3 ~ +10
Supply voltage	AVDD ~ AGND	V	-0.3 ~ +8
Supply voltage	AVEE ~ AGND	V	0.3 ~ -8
Supply voltage	BVDD ~ AGND	V	-0.3 ~ +8
Supply voltage	BVEE ~ AGND	V	0.3 ~ -8
Supply voltage	VGH ~ AGND	V	-0.3 ~ +16
Supply voltage	VGL ~ AGND	V	0.3 ~ -16
Driver supply voltage	AVDD – AVEE	V	≦14V
Driver supply voltage	VGH – VGL	V	≦30V
Input voltage	VIN	V	-0.3 ~ VDDI + 0.3
HS Input voltage	VHSI	V	-0.3 ~ + 2
Operating temperature	Topr	℃	-40 ~ +85
Storage temperature	Tstg	℃	-55 ~ +110

Note:

Even if the one of the above parameters is exceeded momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the exceeding values which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum

8.2 DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage	VDDR VDDA VDDB	-	2.5	2.8	3.3	V	
Operating voltage	VDDI	-	1.65	1.8	3.3	V	Note1,2
OTP Supply voltage	VPP	-		8.0		V	Note1
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE, SDO (SDA) , LEDPWM	VOH	-	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE, SDO (SDA) , LEDPWM	VOL	-	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	9.0	-	16	V	
Gate Driver Low Voltage	VGL	-	-12	-	-8.0	V	
Driver Supply Voltage	-	|VGH-VGL|	17	-	28	V	
DC VCOM Amplitude Voltage	VCOM	FIX GND	0	0-	0	V	Note3
Source Output Range	VSOUT	-	VGMN +0.1	-	VGMP -0.1	V	Note4
Positive Gamma Reference Voltage	VGMP	-	4.5	-	6.5	V	Note5
Negative Gamma Reference Voltage	VGMN	-	-4.5	-	-2.5	V	Note5
Positive Gamma Reference Voltage	VGSP	-	0.7	-	1.8	V	Note5
Negative Gamma Reference Voltage	VGSN	-	0.7	-	1.8	V	Note5

Note:

1. Ta = -30 to 70 °C (to 85 °C no damage), VDDI=1.65V to 3.3V, VDDR VDDA VDDB=2.5V to 3.3V.
2. Supply digital VDDI voltage equal or less than analog VDDR VDDA VDDB voltage.
3. Source channel loading = 10pF/channel
4. The Max. Value is between with Note 3 measure point and Gamma setting value

.

8.3 DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	Low (LP)

Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

8.4 DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage		Operating voltage	2.5	2.8	3.3	V
Digital power supply voltage	VDDI	I/O supply voltage	1.65	1.8	3.3	V
Analog power supply voltage noise	VVDD_NOISE	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	VVDDI_NOISE	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. These values are not symmetric amplitude, which centersm3g points are VDDI or VDD. See examples as reference purposes, when VVDD_NOISE and VVDDI_NOISE are maximums, below.

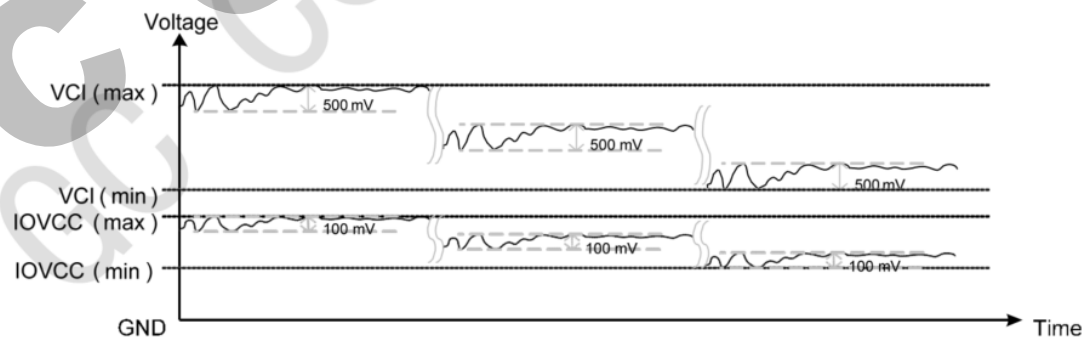


Figure 109 Noise on Power Supply Lines

8.5 DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output	V_{OH}	I_{OUT}=-1mA, Note 2	0.8 V_{VDD}	-	V_{VDD}	V
Logic Low level output	V_{OL}	I_{OUT}=1mA, Note 2	0.0	-	0.2V_{VDD}	V
Logic High level input	V_{IHLPCD}	LP-CD, Note 3	450	-	135	mV
Logic Low level input	V_{ILLPCD}	LP-CD, Note 3	0.0	-	20	mV
Logic High level input	V_{IHLPRX}	LP-RX (CLK, D0 ,D1), Note 3	880	-	135	mV
Logic Low level input	V_{ILLPRX}	LP-RX (CLK, D0 ,D1), Note 3	0.0	-	55	mV
Logic Low level input	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode), Note 3	0.0	-	30	mV
Logic high level output	VOHLPTX	LP-TX (D0), Note 3	1.1	-	1.	V
Logic Low level output	VOLLPTX	LP-TX (D0), Note 3	-50	-	5	mV
Logic High level input	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. LEDPWM
3. DSI High Speed mode is off

8.6 Spike / Glitch Rejection

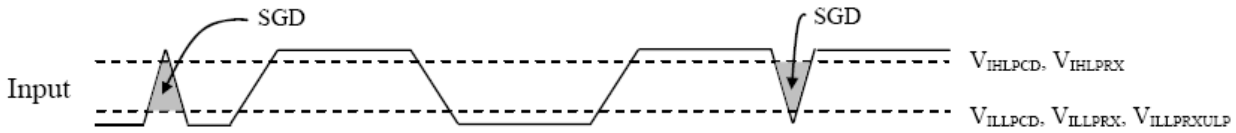


Figure 110 Spike / Glitch Rejection

Note:

1. Peak Interference Amplitude max. 200mV and Interference Frequency min. 450MHz.
2. n = 0 and 1.

Table 44 Spike / GlitchRejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
Input pulse rejection for DSI	SGD	Input pulse rejection for DSI	-	300	Vps

8.7 DC Characteristics for DSI HS mode

Parameter	Symbol	Conditi	Specification			Unit
Input Common Mode Voltage for Clock	VCMCLK	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	VCMDATA	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	VCMRCLKL450	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	VCMRDATAL450	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine	VCMRCLKM450	DSI-CLK+/-	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	VCMRDATAM450	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	VTHLCLK-	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	VTHLDATA-	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	VTHHCLK+	DSI-CLK+/-	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	VTHHDATA+	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	VILHS	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	VIHHS	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	RTERM	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	VTERM-EN	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	CTERM	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

1. Ta = -30℃ to 70℃ (to +85℃ no damage), VDDI = 1.65 to 1.95V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.

4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0 and 1.
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification

The DSI receiver (HS mode) is understanding that there is logical ‘1’ (HS-1) when a differential voltage is more than VTHH (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical ‘0’ (HS-0) when a differential voltage is more than VTHL (CLK-/DATA-). There is undefined state if the differential voltage is less than VTHH (CLK+/DATA+) and less than VTHL (CLK-/DATA-). A reference figure is below.

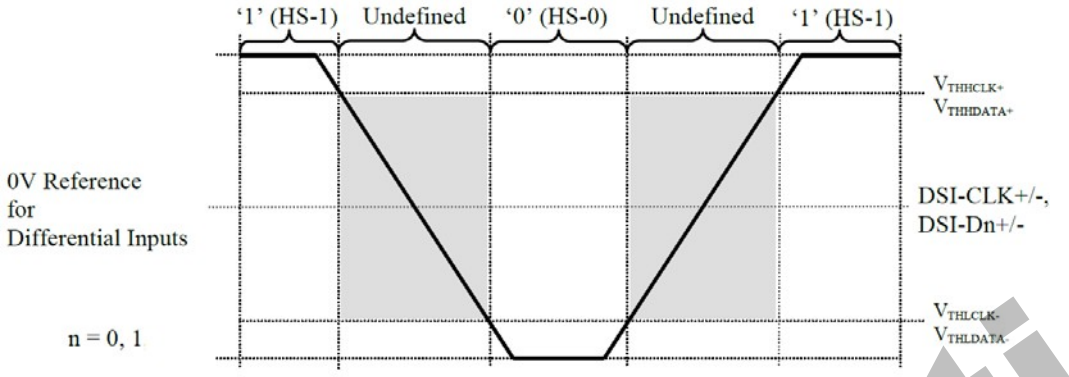
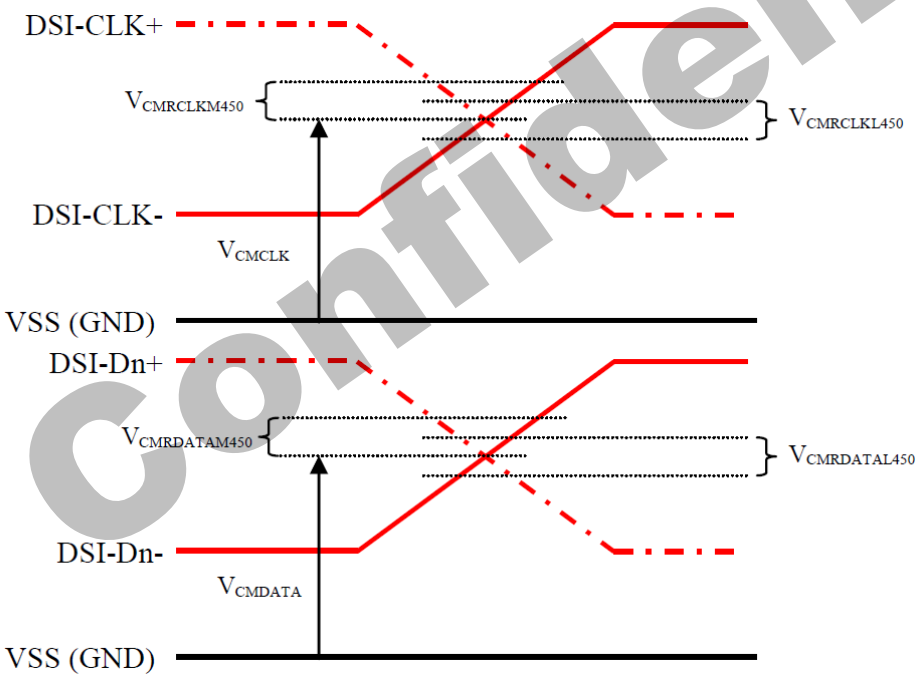


Figure 111 Differential Inputs Logical ‘0’s and ‘1’s, Threshold High/Low, Differential Voltage Range



Note: n = 0 and 1

Figure 112 Common Mode Voltage on Clock and Data Channels

The termination resistor (RTERM) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs
  (DSI-CLK+ Ù DSI-CLK- or DSI-D0+ Ù DSI-D0- or DSI-D1+ Ù DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs
  (DSI-CLK+ Ù DSI-CLK- or DSI-D0+ Ù DSI-D0- or DSI-D1+ Ù DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

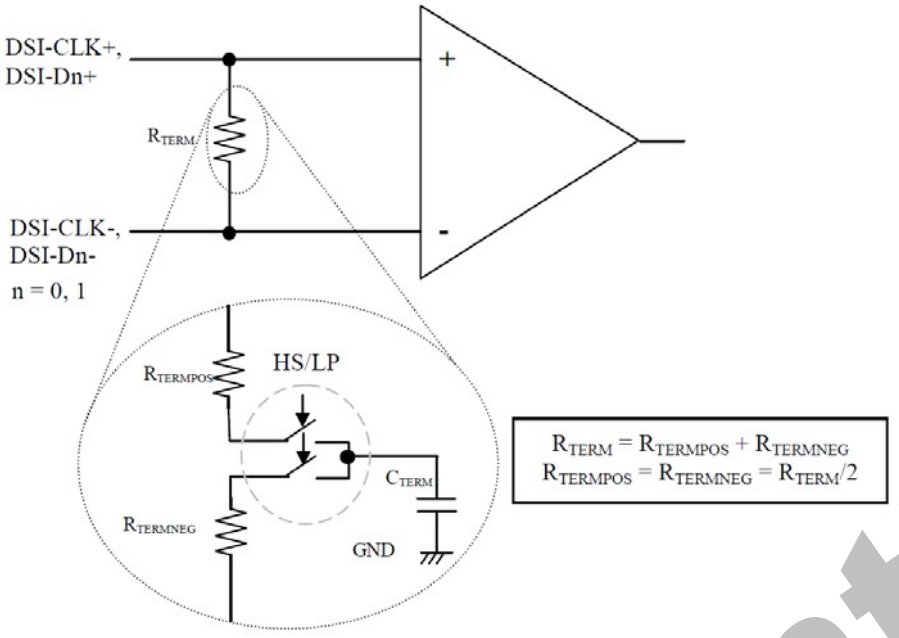
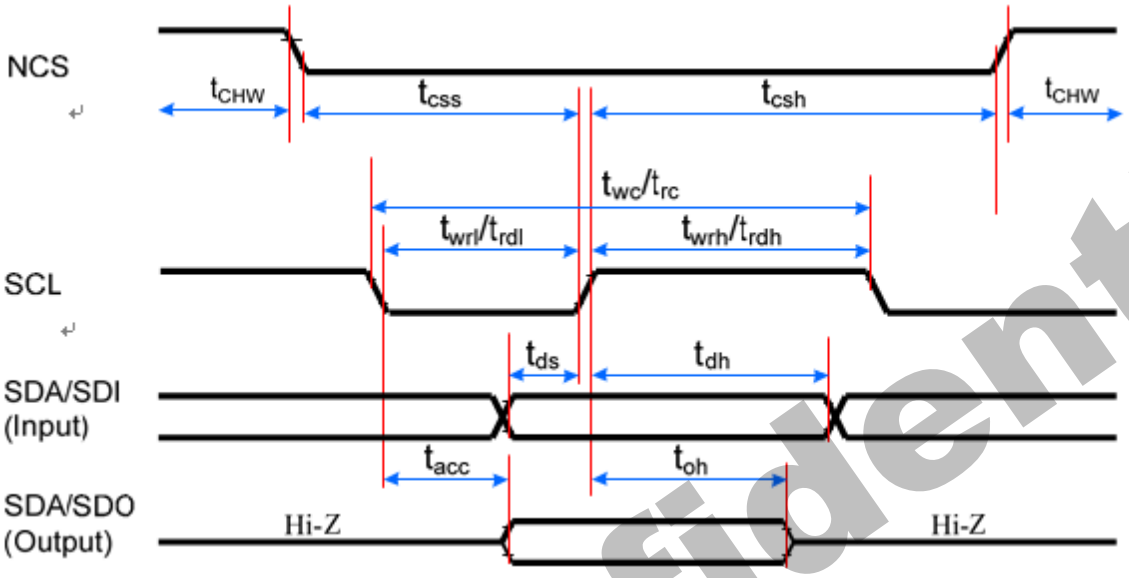


Figure 113 Differential Pair Termination Resistor on the Receiver Side

8.8 AC Characteristics

8.8.1 Display Serial Interface Timing Characteristics (3-line SPI system)

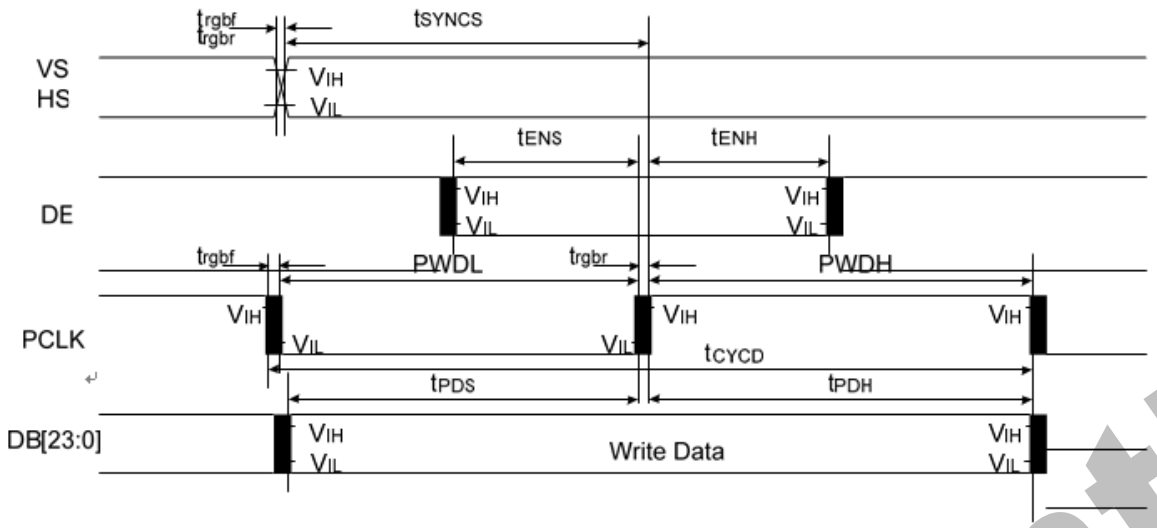


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

8.8.2 .Parallel 24/18/16-bit RGB Interface Timing



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	tSYNCS	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	tSYNCH	VS/HS hold time	5	-	ns	
DE	tENS	DE setup time	5	-	ns	
	tENH	DE hold time	5	-	ns	
DB[23:0]	tPOS	Data setup time	5	-	ns	
	tPDH	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	tCYCD	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, DGND=0V

8.8.3 DSI Timing Characteristics

8.8.3.1 High Speed Mode – Clock Channel Timing

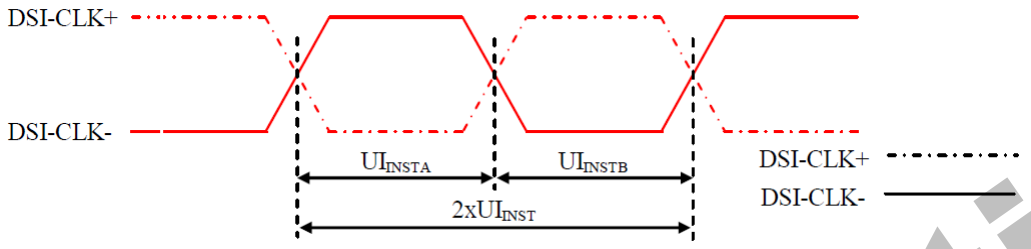


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UIINSTA,UIINSTB	UI instantaneous Half	2	12.5	ns

Note: UI = UIINSTA = UIINSTB

8.8.3.2 High Speed Mode – Data Clock Channel Timing

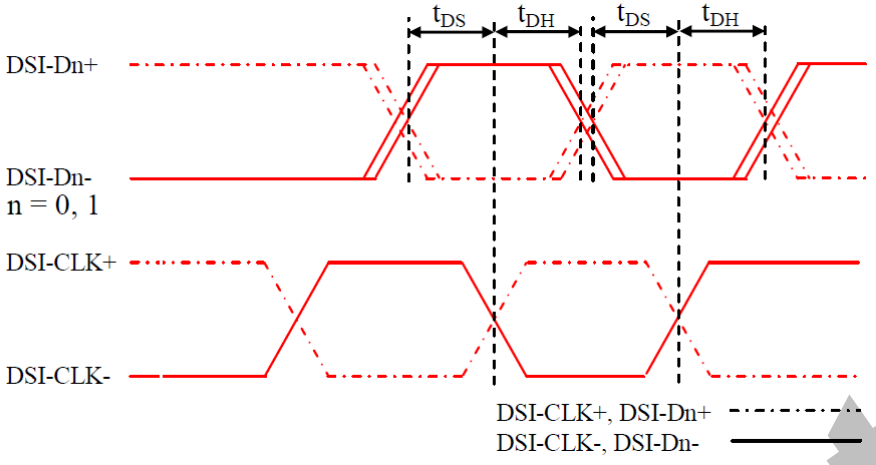


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	tDS	Data to Clock Setup time	0.15x UI	-
	tDH	Clock to Data Hold Time	0.15x UI	-

8.8.3.3 High Speed Mode – Rise and Fall Timings

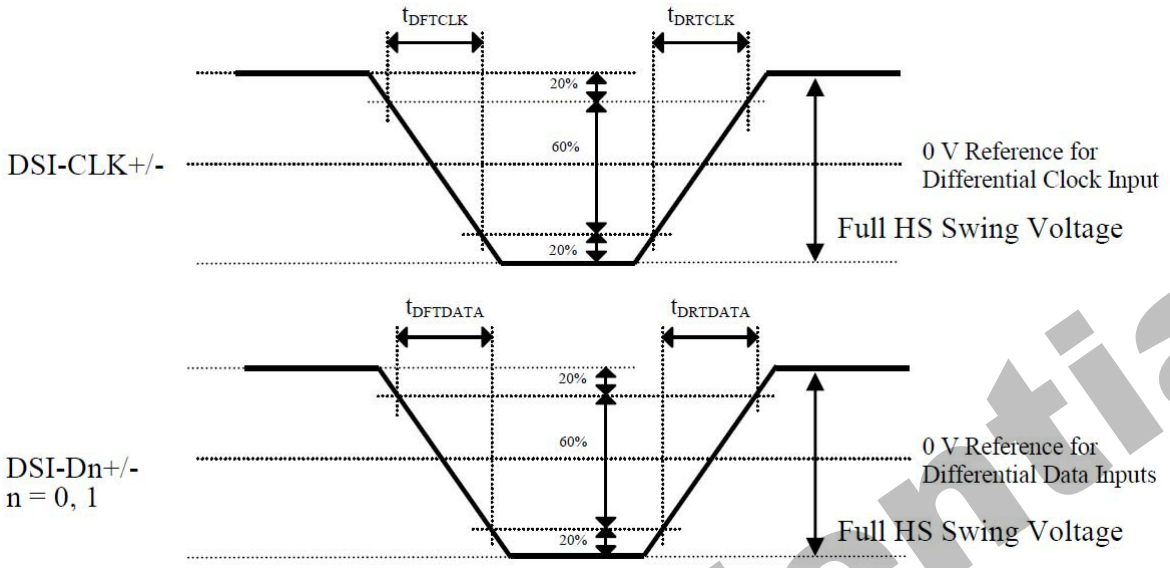


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	tDRTCLK	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	tDRTDATA	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	tDFTCLK	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	tDFTDATA	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

8.8.3.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9503NP) sequence below.

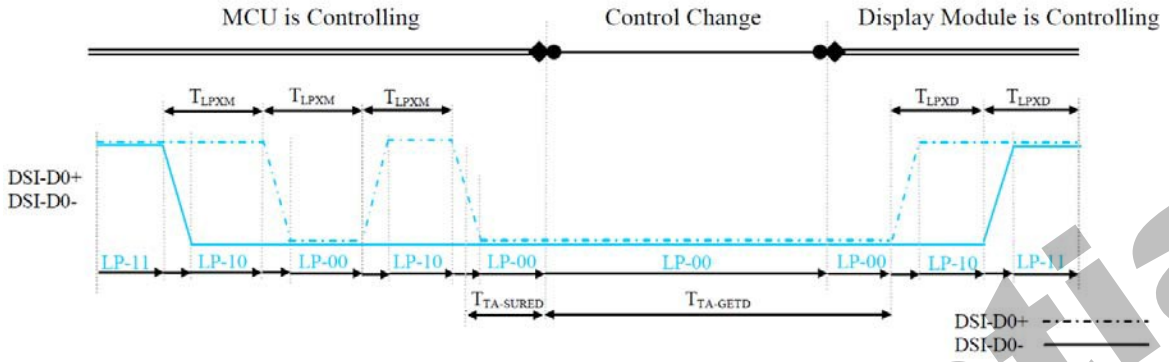


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (GC9503NP) to the MPU sequence below.

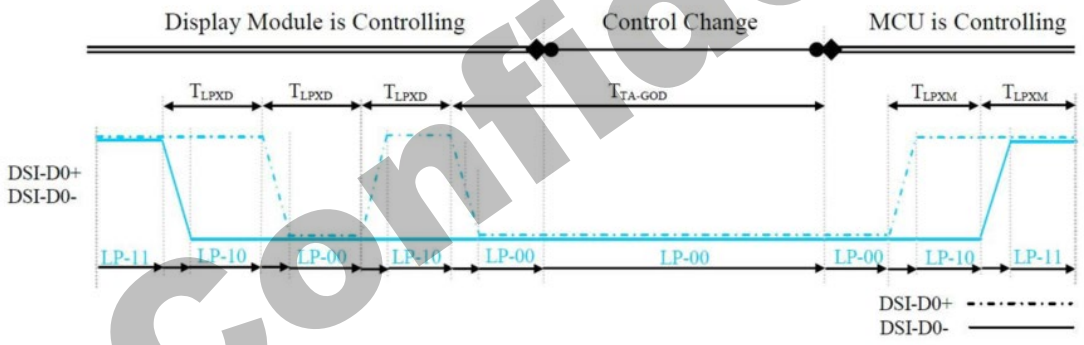


Figure 118 BTA from the Display Module to the

MPU Table 48 Low Power State Period Timings – A

Sign	Symbol	Description	Min	Max	Unit
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ⇑ Display Module (GC9503NP)	50	75	ns
DSI-D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (GC9503NP) ⇑ MPU	50	75	ns
DSI-D0+/-	TTA-SURED	Time-out before the Display Module (GC9503NP) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by Display Module (GC9503NP)	$5\times T_{LPXD}$	ns
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	$4\times T_{LPXD}$	ns

8.8.3.5 Data Lanes from Low Power Mode to High Speed Mode

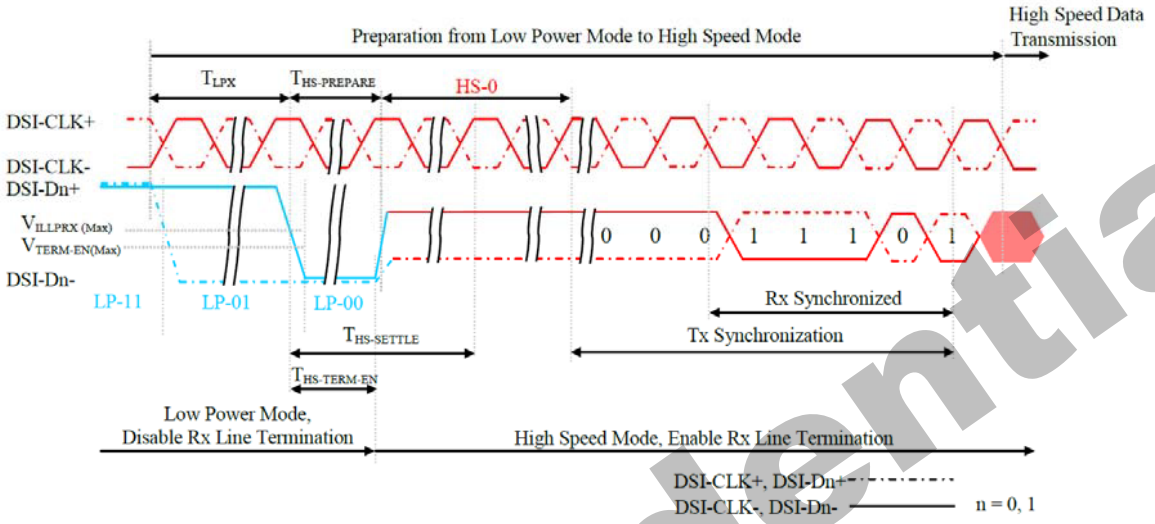


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	TLPX	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	THS-TERM-EN	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

8.8.3.6 Data Lanes from High Speed Mode to Low Power Mode

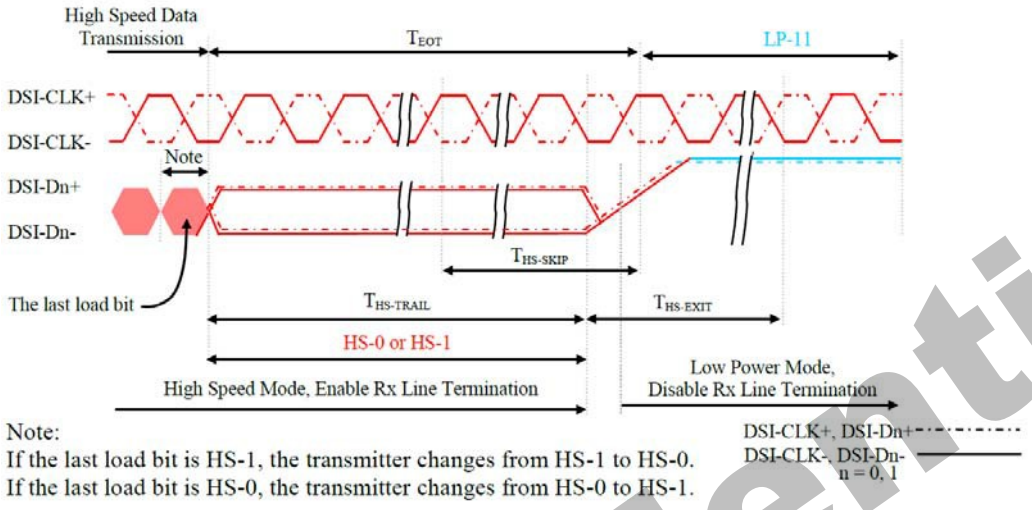


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	THS-SKIP	Time-Out at Display Module (GC9503NP) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	THS-EXIT	Time to driver LP-11 after HS burst	100	-	ns

8.8.3.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

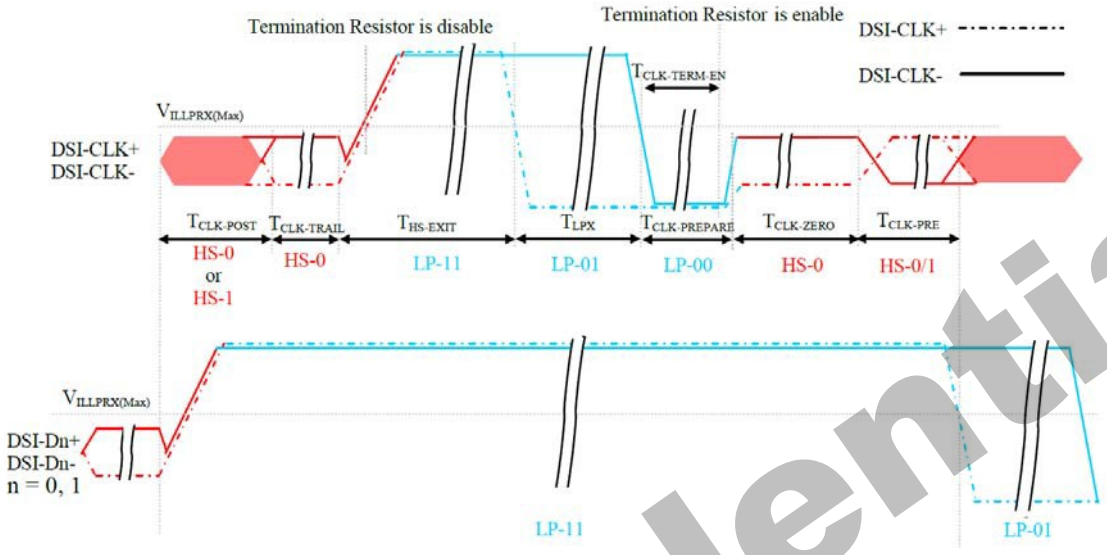


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	TCLK-POST	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	TCLK-TERM-EN	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	TCLK-PREPARE	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns